

8

7

6

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4

3

2

1

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.

2. ALL CAPACITANCE VALUES ARE IN MICROFARADS

3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV

ECN

DESCRIPTION OF REVISION

CK APPD

DATE

B

0003279770

PRODUCTION RELEASED

2014-09-29

http://www.xinxunwei.com TEL:0755-61506416 QQ:1727176051 981775188

MLB B - PVT

LAST\_MODIFIED=Mon Sep 29 18:09:18 2014

RADIO\_MLB SYNC VER 0.109.0

WIFI\_DEV SYNC VER 0.68.0

ROTTERDAM SYNC VER 0.11.0

PDF CSA CONTENTS

SYNC MASTER

DATE

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N/A

N/A

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BLOCK DIAGRAM: SYSTEM

N/A

N/A

3

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BOM TABLES

N/A

N/A

4

5

SOC: MISC & ALIASES

N/A

N/A

5

6

SOC: MAIN

N/A

N/A

6

7

SOC: I/OS

N/A

N/A

7

8

SOC: NAND

N/A

N/A

8

9

SOC: MIPI, ISP

N/A

N/A

9

10

SOC: EDP, PCIE

N/A

N/A

10

11

SOC: DDR

N/A

N/A

11

12

SOC: IO POWER

N/A

N/A

12

13

SOC: SOC POWER AND GND

N/A

N/A

13

14

SOC: CPU, GPU, SRAM POWER

N/A

N/A

14

16

DDR: CHANNEL 0 AND 1

N/A

N/A

15

17

DDR: CHANNEL 2 AND 3

N/A

N/A

16

18

NAND

N/A

N/A

17

20

SENSOR: OSCAR

N/A

N/A

18

21

SENSOR: CARBON, PHOS+, MAGN

N/A

N/A

19

22

SENSOR: HALL EFFECT

N/A

N/A

20

27

CAMERA: CAM CONNS

N/A

N/A

21

28

CAMERA: CAM SUPPORT

N/A

N/A

22

30

AUDIO: L81 CODEC

N/A

N/A

23

31

AUDIO: HP/DMIC FLEX CONNS

N/A

N/A

24

32

AUDIO: SPEAKER AMPS

N/A

N/A

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IO: TRISTAR

N/A

N/A

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IO: FILTERS

N/A

N/A

27

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IO: HOTBAR PADS

N/C

N/A

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IO: BUTTON FLEX CONN

N/A

N/A

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40

GRAPE: STINGER & CONN

N/A

N/A

30

41

GRAPE: CUMULUS

N/A

N/A

31

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DISPLAY: CONNECTOR

N/A

N/A

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DISPLAY: EDP SUPPORT

N/A

N/A

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MESA: SUPPORT

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ROTTERDAM

05/13/2014

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N/A

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PMU: ARABELA (1/3)

N/A

N/A

61

82

PMU: ARABELA (2/3)

N/A

N/A

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83

PMU: ARABELA (3/3)

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N/A

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POWER: J82 SPECIFIC

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N/A

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POWER: EXTERNAL SWITCHES

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PMU: CHARGER BUCK

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POWER: BATTERY CONN

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N/A

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SOC: DEBUG

N/A

N/A

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ALIASES: BB/WLAN/BT

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TEST: TPS/HOLES/FIDUCUALS

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N/A

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TEST: EE TP/PP

N/A

N/A

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TEST: CELL EE TP/PP

N/A

N/A

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N/A

N/A

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BB/WLAN VOLTAGE ATTRIBUTES

N/A

N/A

DRAWING

SCH AND BOARD P/N

PART#

QTY

DESCRIPTION

REFERENCE DESIGNATOR(S)

CRITICAL

BOM OPTION

051-0301

1

SCH\_MLB-B\_J82

SCH1

CRITICAL

051-362

1

SCHEM\_MLB-B\_J82

PCB1

CRITICAL

DRAWING TITLE

SCHEM,MLB-B,X190

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SIZE

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REVISION

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BRANCH

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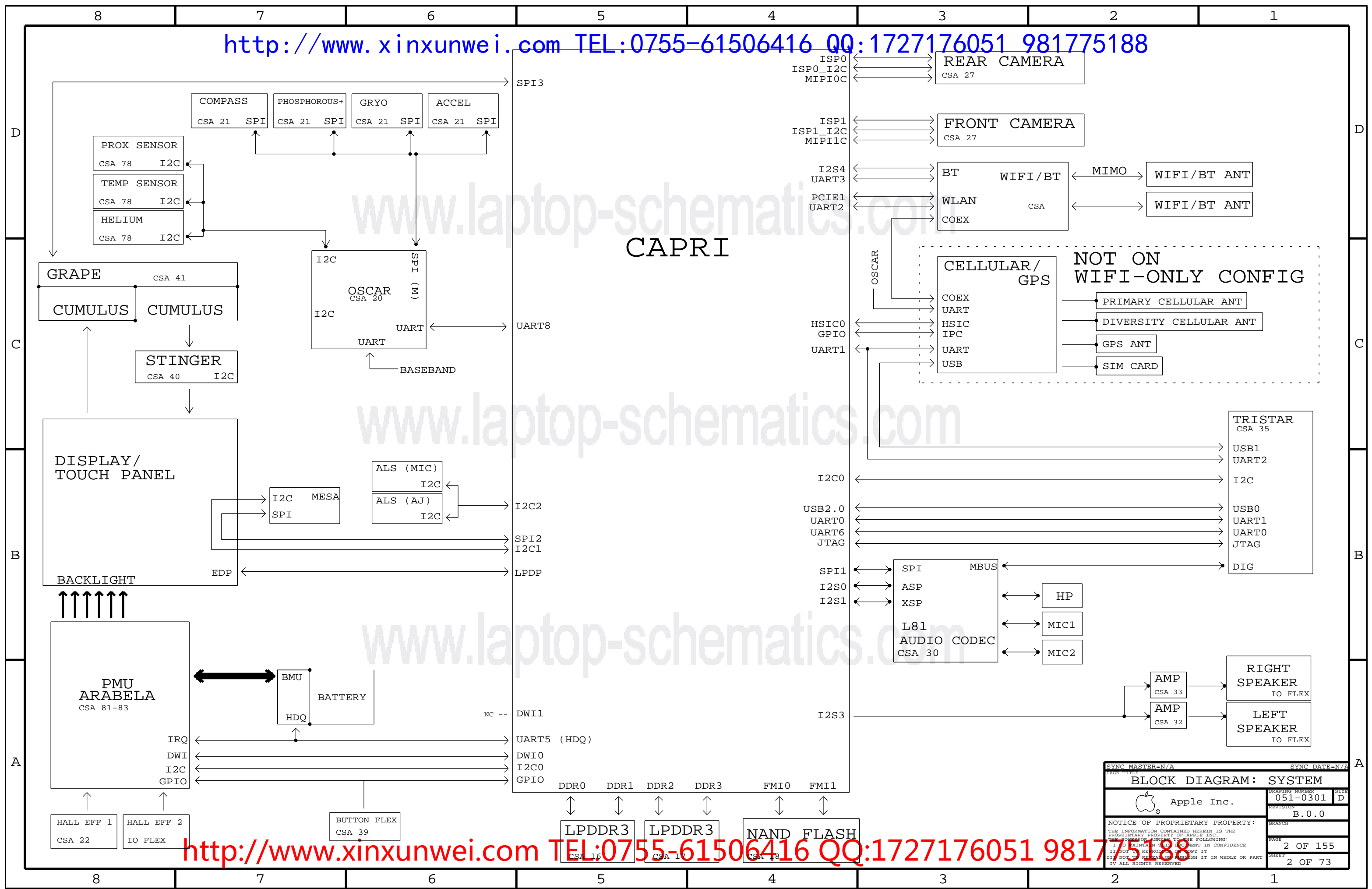
4

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Page Notes

Power aliases required by this page: (NONE)
Signal aliases required by this page: (NONE)
BOM options provided by this page:

SOC

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S00016	1	IC,CAPRI,A1,PROD,ASE	U0600	CRITICAL	
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
343S00021	343S00016		U0600	IC,CAPRI,A1,PROD,SCK	

PMU

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0675	1	IC,PMU,ARABELLA,D2207A0,TOP-AC,FCBGA380	U8100	CRITICAL	

SDRAM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S0803	2	IC,CAPRI,DRAM,10X10MM,FBGA261	U1600,U1700	CRITICAL	
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
333S0804	333S0803		U1600,U1700	ELPIDA DRAM	
333S00014	333S0803		U1600,U1700	SAMSUNG DRAM	

NAND

16GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S0972	1	TOSHIBA 16GB MLC 1YNM PPN1.5	U1800	CRITICAL	16GB_PROD
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
335S1035	335S0972	16GB_PROD	U1800	HYNIX 16GB MLC 1YNM PPN1.5	

64GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S00011	1	SANDISK 64GB TLC 1YNM PPN1.5	U1800	CRITICAL	64GB_PROD
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
335S00017	335S00011	64GB_PROD	U1800	TOSHIBA 64GB TLC 1YNM PPN	

128GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S00012	1	SANDISK 128GB TLC 1YNM PPN1.5	U1800	CRITICAL	128GB_PROD
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
335S00018	335S00012	128GB_PROD	U1800	TOSHIBA 128GB TLC 1YNM PPN	

MECHANICAL PARTS


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
806-7118	1	RADIO FENCE X190	PD_FENCE_RADIO	CRITICAL	MLB_B
806-00001	1	AP FENCE X190	PD_FENCE_AP	CRITICAL	
806-6353	1	GRAPE FENCE X190	PD_FENCE_GRAPE	CRITICAL	

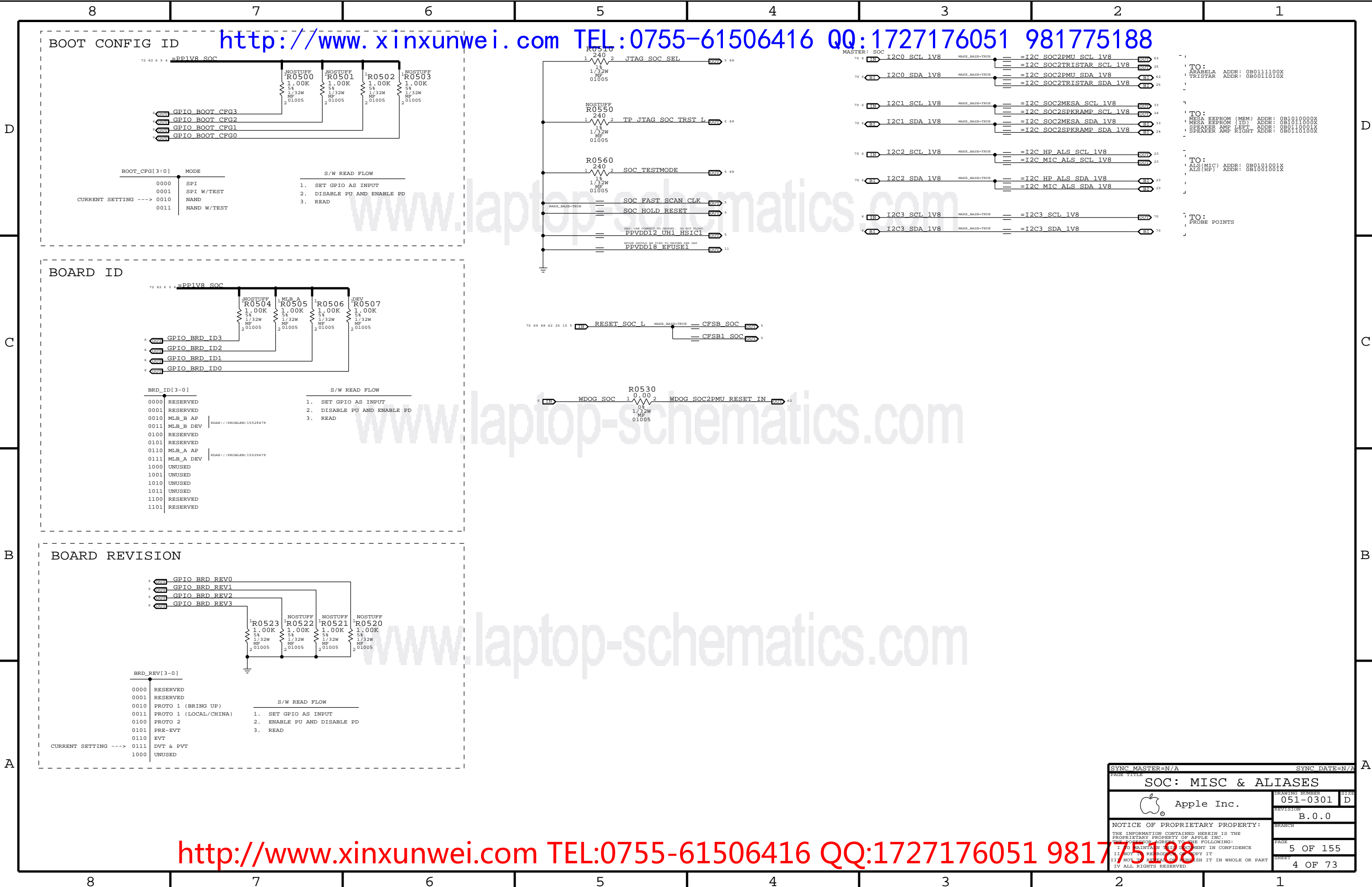
BARCODE LABEL/EEEE CODES

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-00067	1	EEEE FOR 639-5813 (MLB A 16GB)	EEEE_FQJ3	CRITICAL	EEEE_MLB_A_16GB
825-00067	1	EEEE FOR 639-5814 (MLB A 32GB)	EEEE_FQJ0	CRITICAL	EEEE_MLB_A_32GB
825-00067	1	EEEE FOR 639-5815 (MLB A 64GB)	EEEE_FQJ1	CRITICAL	EEEE_MLB_A_64GB
825-00067	1	EEEE FOR 639-5816 (MLB A 128GB)	EEEE_FQJ2	CRITICAL	EEEE_MLB_A_128GB
825-00067	1	EEEE FOR 639-4747 (MLB B 16GB)	EEEE_PH54	CRITICAL	EEEE_MLB_B_16GB
825-00067	1	EEEE FOR 639-5809 (MLB B 32GB)	EEEE_FQHY	CRITICAL	EEEE_MLB_B_32GB
825-00067	1	EEEE FOR 639-5810 (MLB B 64GB)	EEEE_FQHW	CRITICAL	EEEE_MLB_B_64GB
825-00067	1	EEEE FOR 639-5811 (MLB B 128GB)	EEEE_FQHV	CRITICAL	EEEE_MLB_B_128GB

CKPLUS WAIVE TABLE

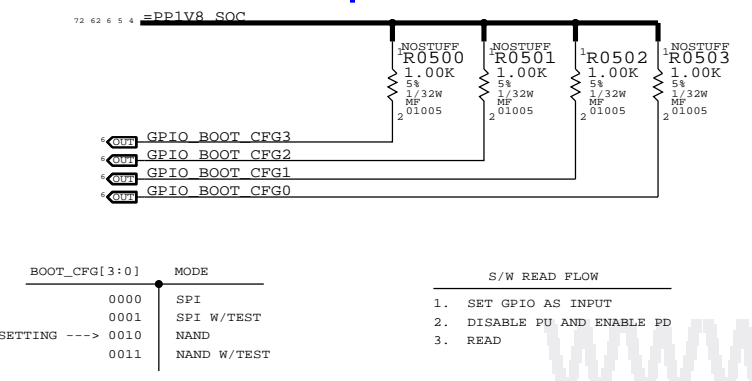
CKPLUS RULE EXCEPTIONS	REQUIRED
SCHEMATIC DEFINED CONSTRAINTS (YES/NO)	NO

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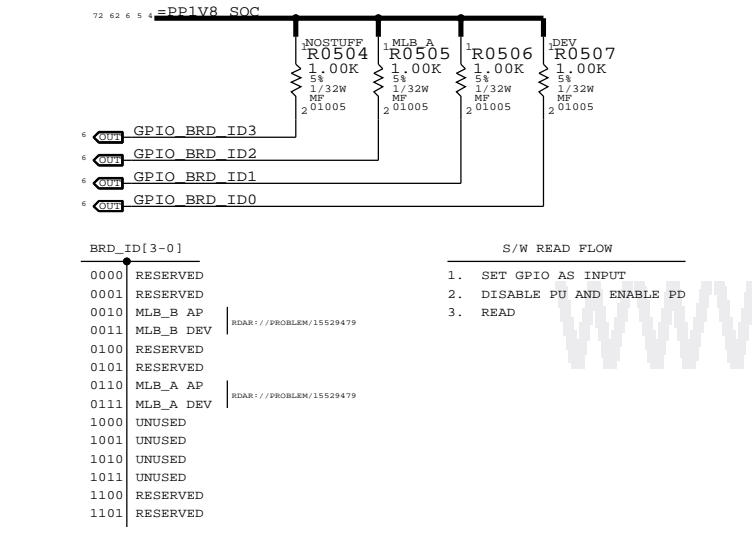


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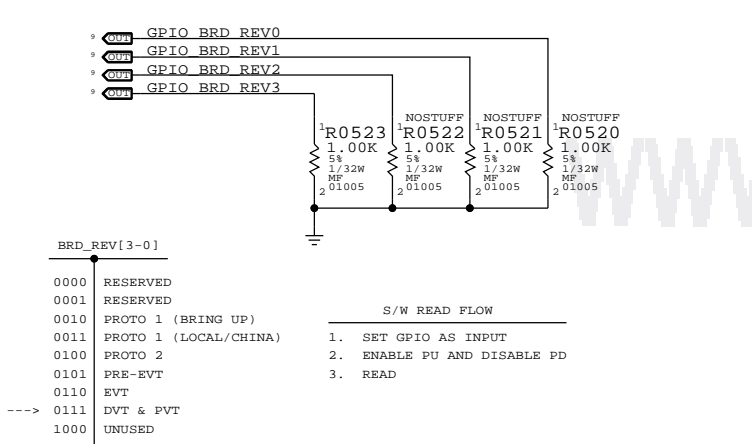
BOOT CONFIG ID



BOARD ID



BOARD REVISION

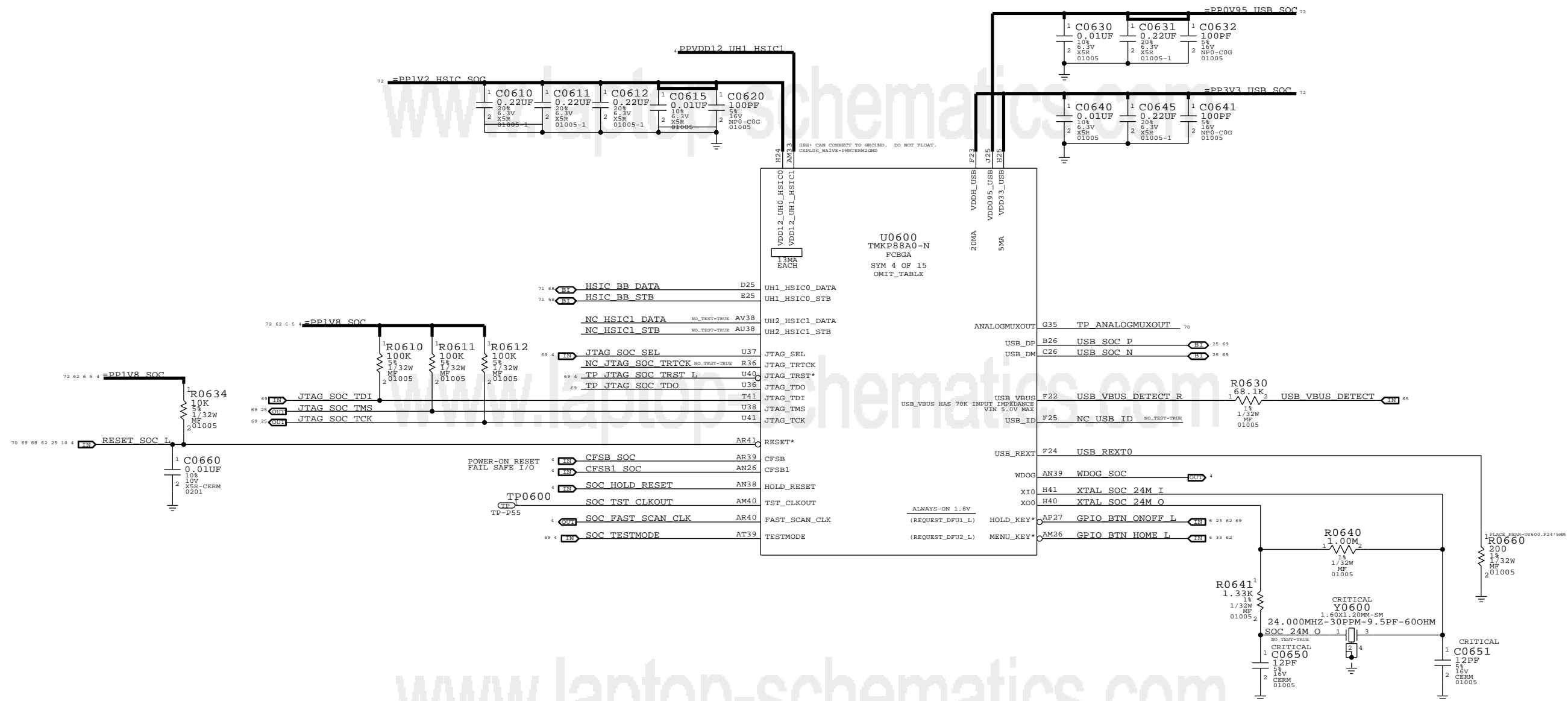


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Apple Inc.		DRAWING NUMBER	051-0301
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ON IN HIBERNATE  
VDD1, VDD2, VDDIOD\_DDRXCA (VDDCA), VDD12\_CKE\_DDR0, VDD12\_CKE\_DDR1

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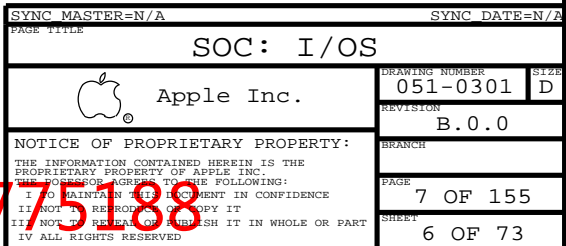
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R_RPU AND R_RPD 45 K OHM
V_NOM 1.8V
V_MAX 1.95V

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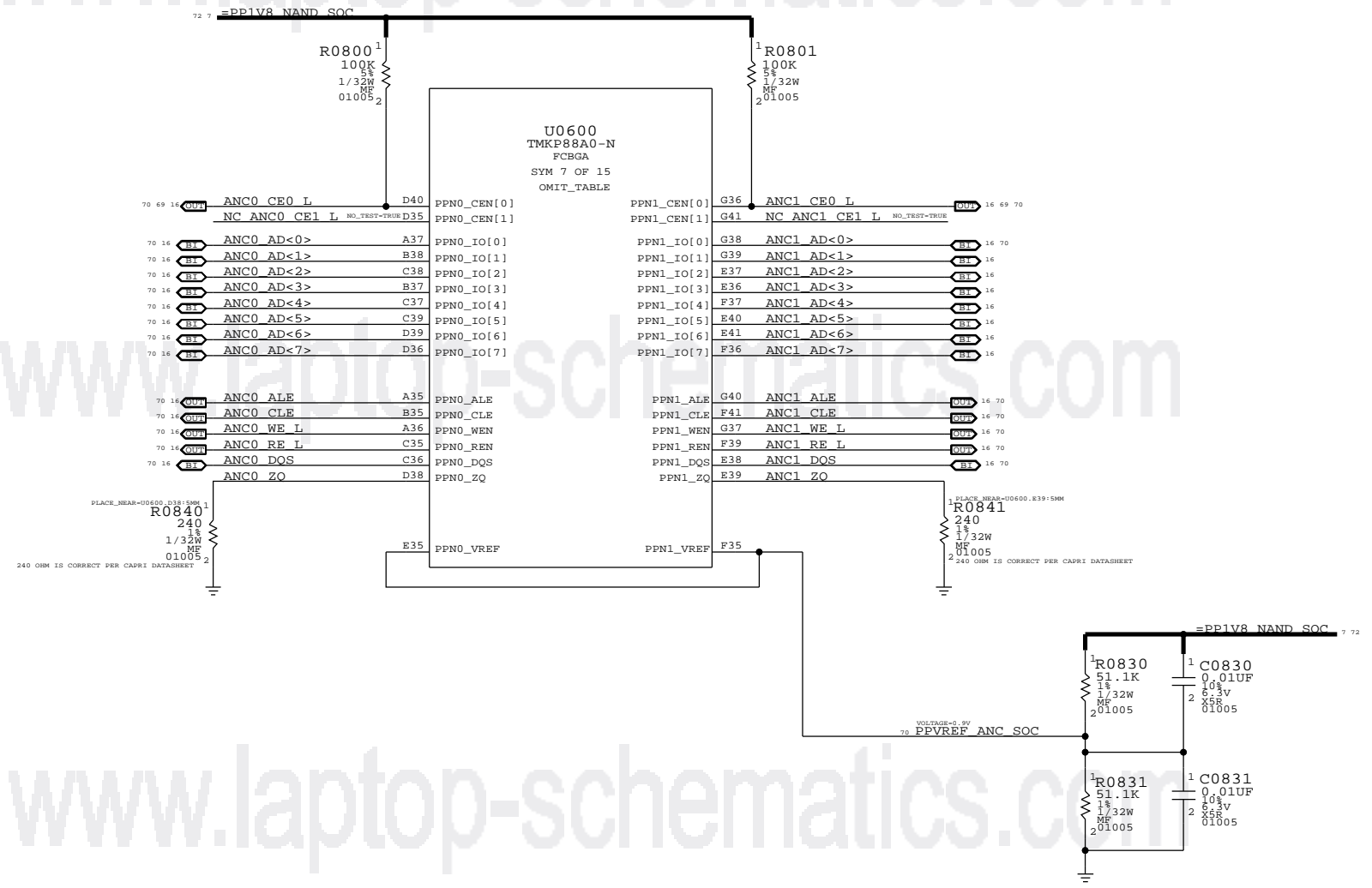



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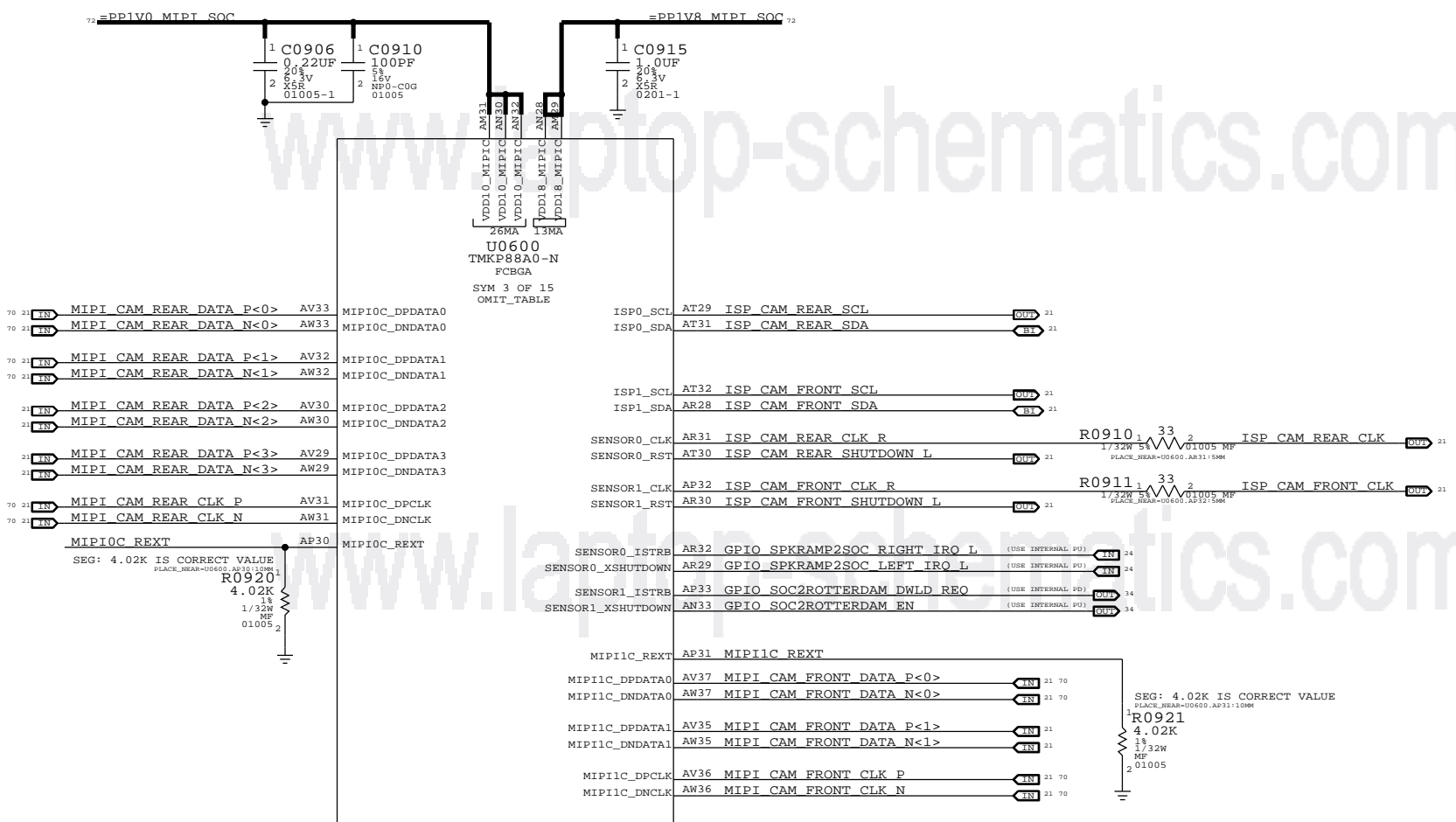
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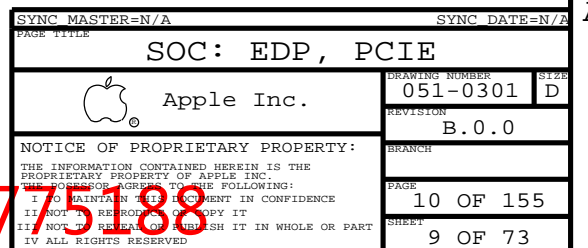
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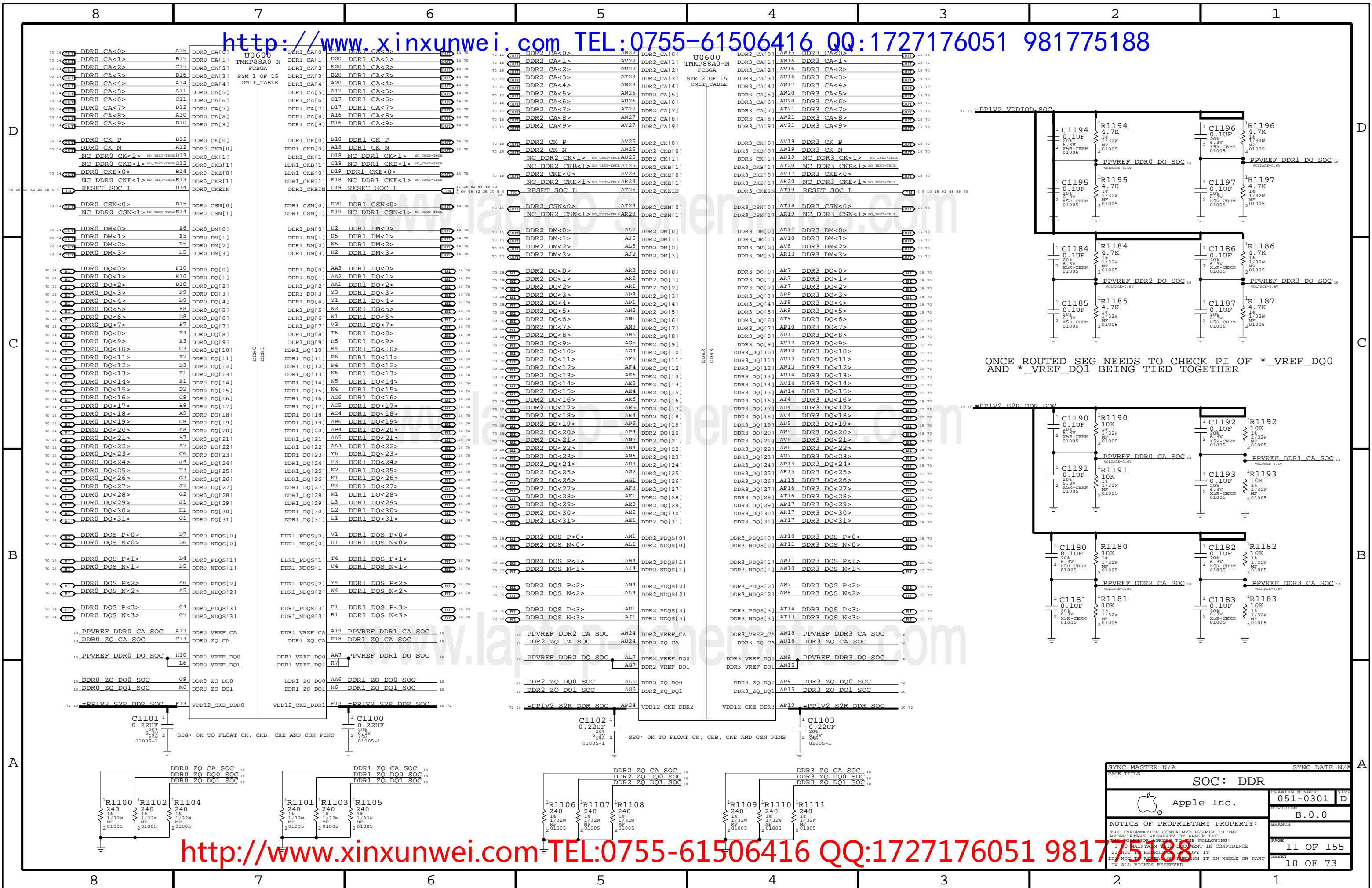
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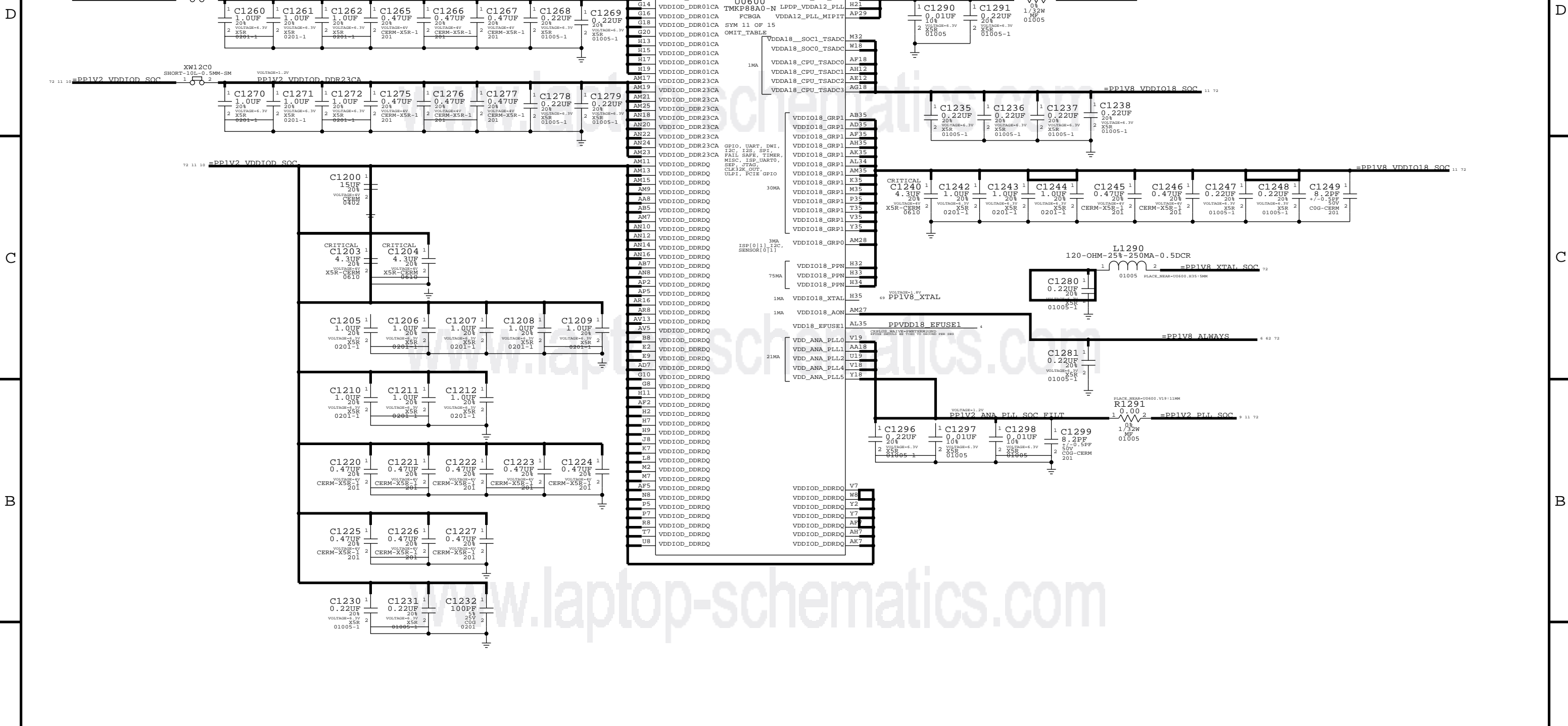
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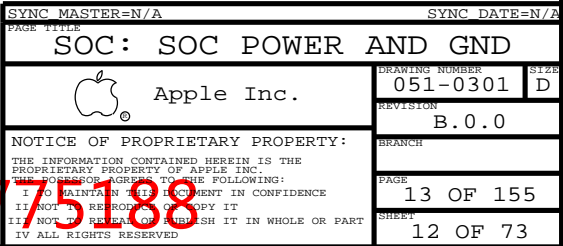
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	SOC PD PARTITIONS	0.904V - 0.996V, 4.0A MAX.	D_SOC	VDD_SOC	K25	AA17	VSS	AE9	AL29	VSS	AU34	F11	VSS
D_SOC	VDD_SOC	K31	AA19	VSS	AF10	AL3	VSS	AU35	F12	VSS			
D_SOC	VDD_SOC	K33	AA21	VSS	AF12	AL31	VSS	AU36	F14	VSS			
D_SOC	VDD_SOC	K9	AA23	VSS	AF14	AL33	VSS	AU37	F15	VSS			
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D_SOC	VDD_SOC	L10	AA27	VSS	AF22	AL40	VSS	AU41	F19	VSS			
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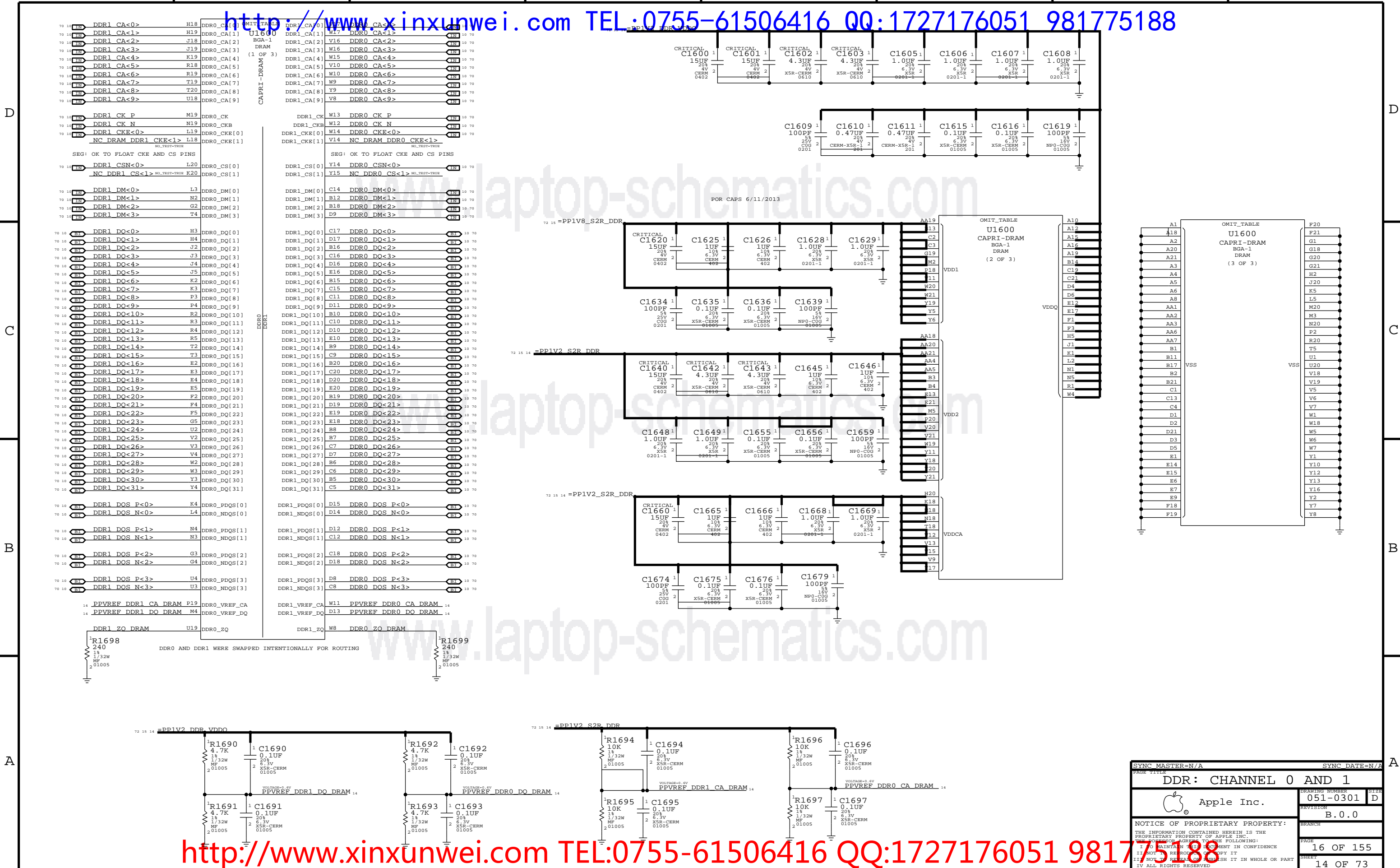
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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
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SOC: CPU, GPU, SRAM POWER		14 OF 155	
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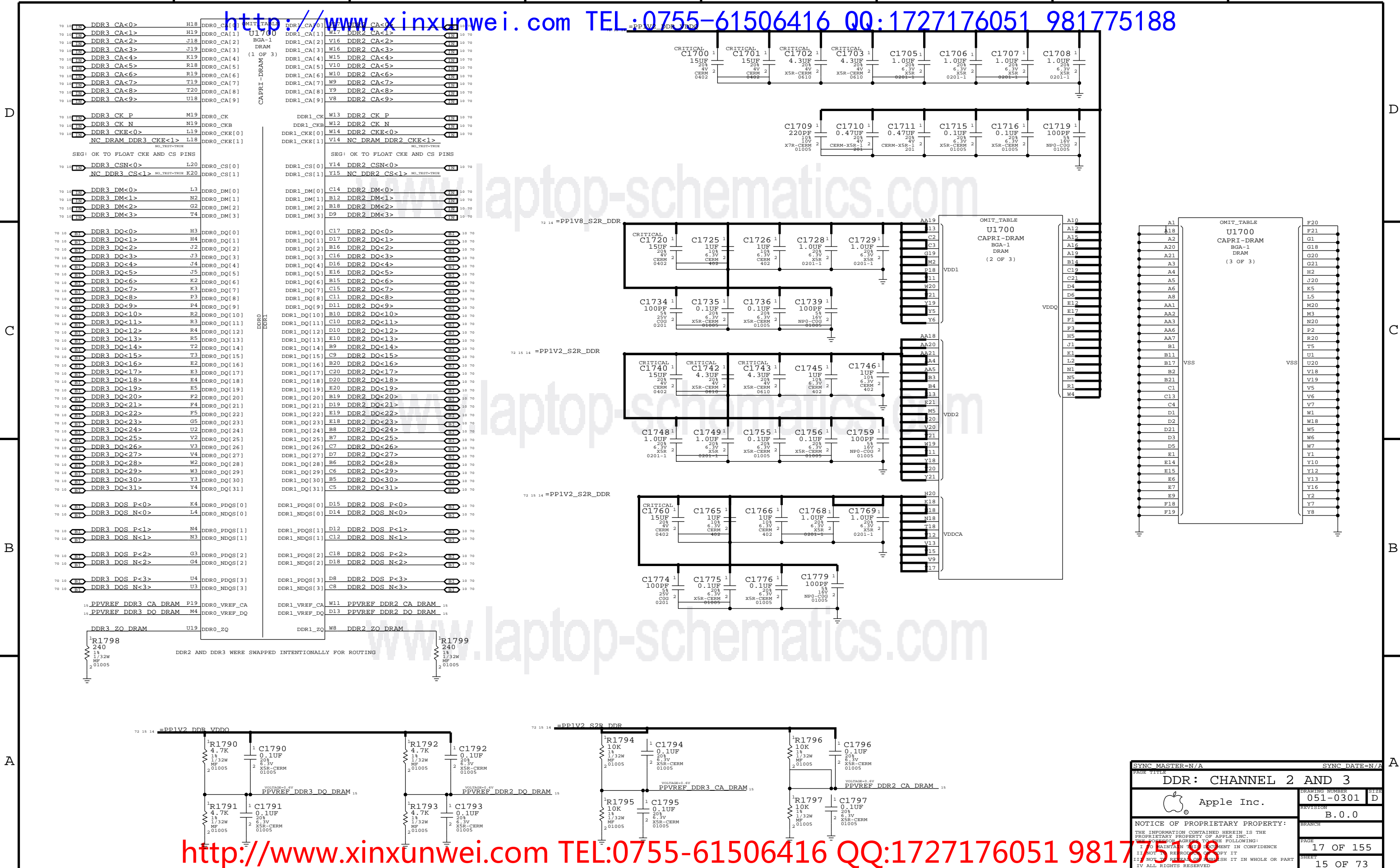


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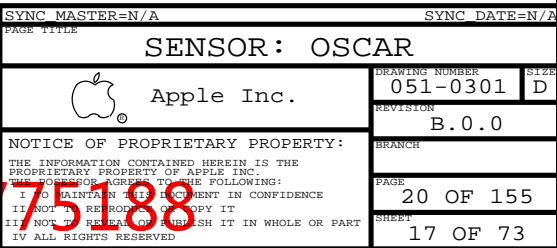


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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S00016	155S0686		FL2000 & MORE	RDAR://PROBLEM/15809407



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# SENSORS

[illegible][illegible]

APN: 338S1014

FL2140

120-OHM-25%-250MA-0.5DCR

VOLTAGE=3.0V

PP3V0 COMPASS

01005

C2142 1.0UF 20A 6.3V X5R-CERM 0201-1

C2140 0.1UF 20A 6.3V X5R-CERM 01005

U2140 AK8963C CSP

VDD VID

VSS

SHORT-10L-0.25MM-SM

XW2140

VOLTAGE=3V

GND COMPASS

FL2141

120-OHM-25%-250MA-0.5DCR

VOLTAGE=1.8V

PP1V8 COMPASS

01005

C2141 0.1UF 20A 6.3V X5R-CERM 01005

GND COMPASS

D1 CAD0 SCL/SK A3 SPI OSCAR2COMPASS SCLK R

D2 CAD1 SDA/SI A4 SPI OSCAR2COMPASS MOSI

NC X2 TST1 CSB\* A2 SPI OSCAR2COMPASS CS L

NC X3 RSV SO B4 SPI COMPASS MISO R

C3 TRG DRDY A1 GPIO COMPASS2OSCAR IRO

D4 RST\* VSS

R2141 150 01005 1% PLACE\_NEAR=U2140, A3:200H

R2142 33 01005 5% PLACE\_NEAR=U2140, B4:200H

GPIO OSCAR2COMPASS TRIGGER

PP1V8 COMPASS

SPI OSCAR2COMPASS SCLK


SPI OSCAR2COMPASS MOSI

SPI OSCAR2COMPASS CS L

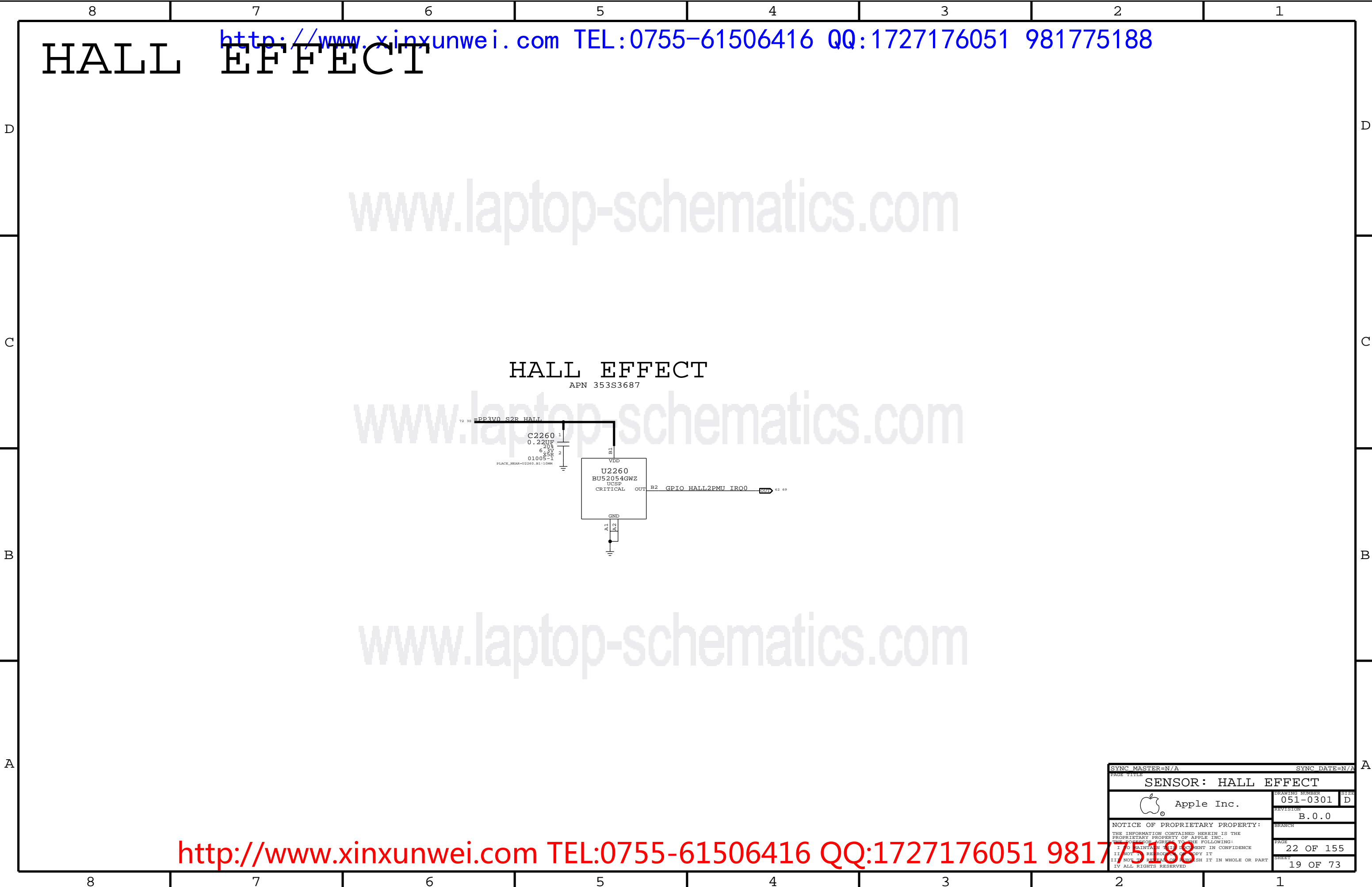
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SPI SENSORS MISO


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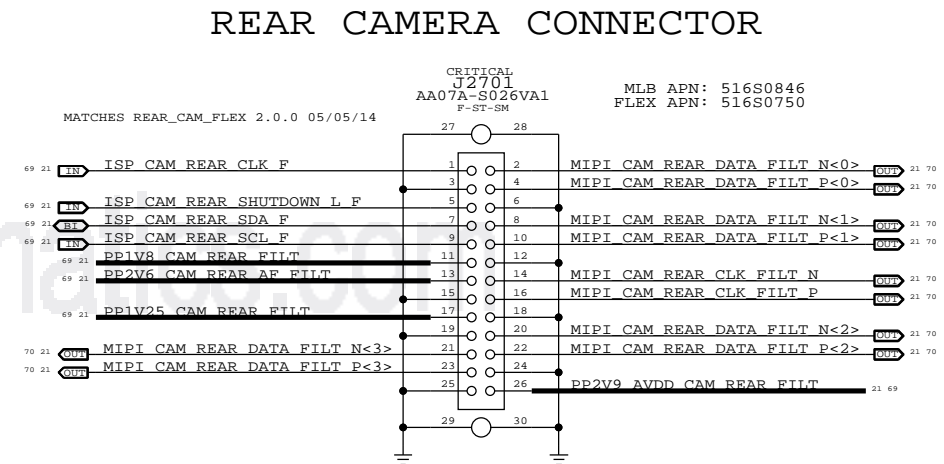
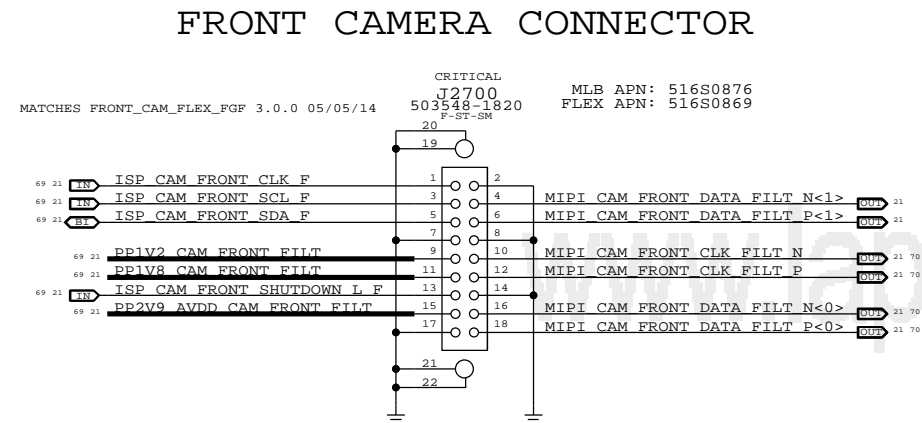
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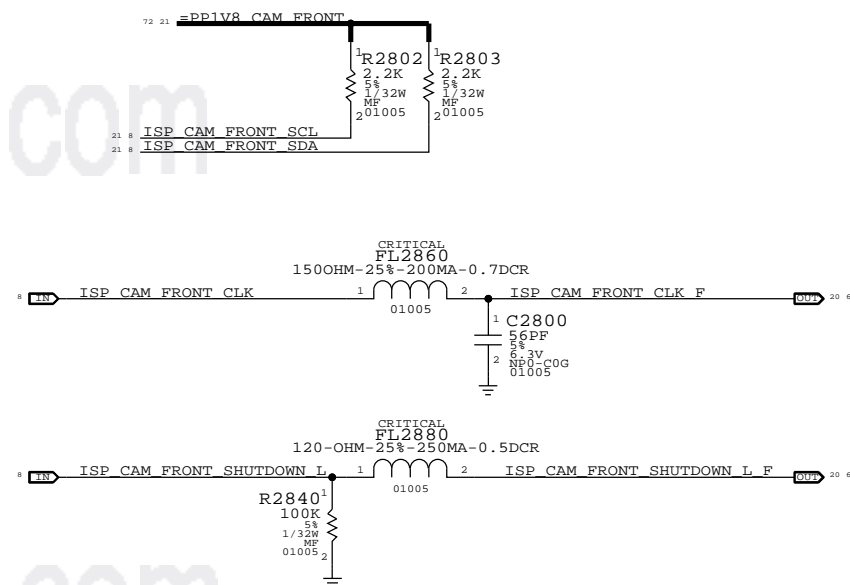
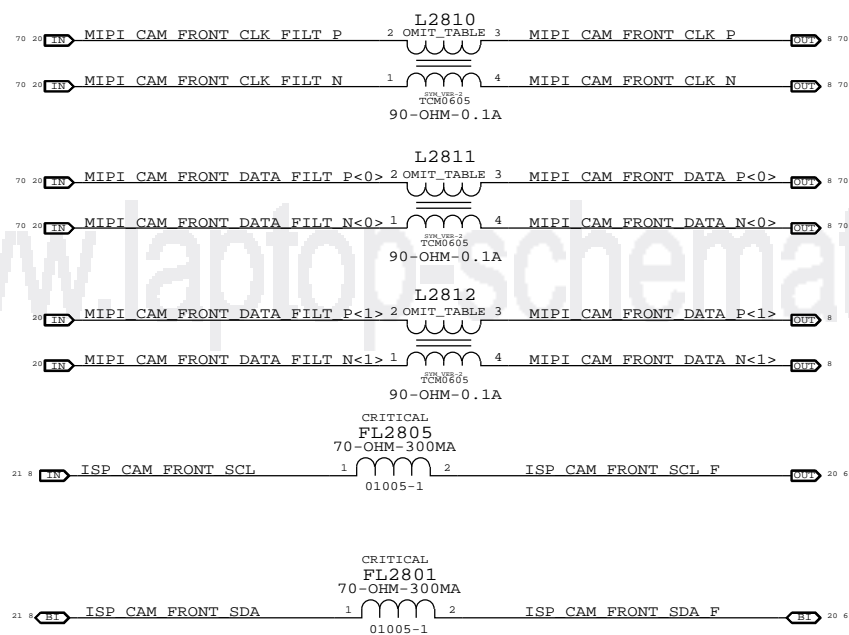
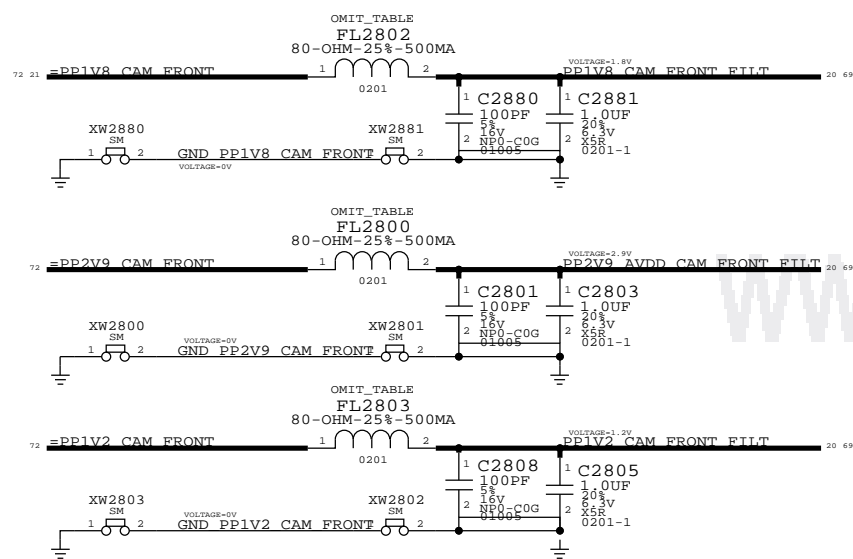
FRONT & REAR CAMERA CONNECTORS



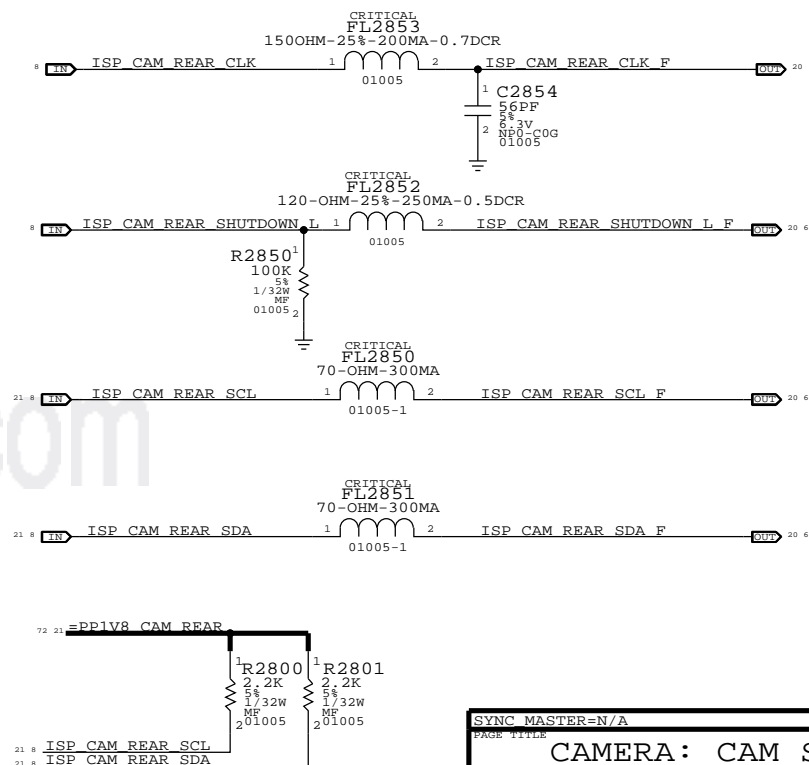
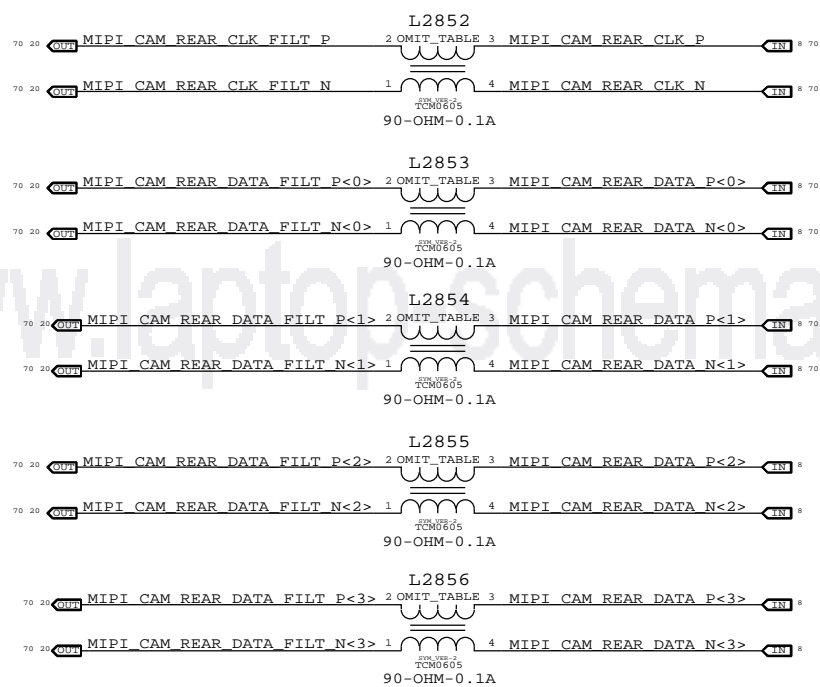
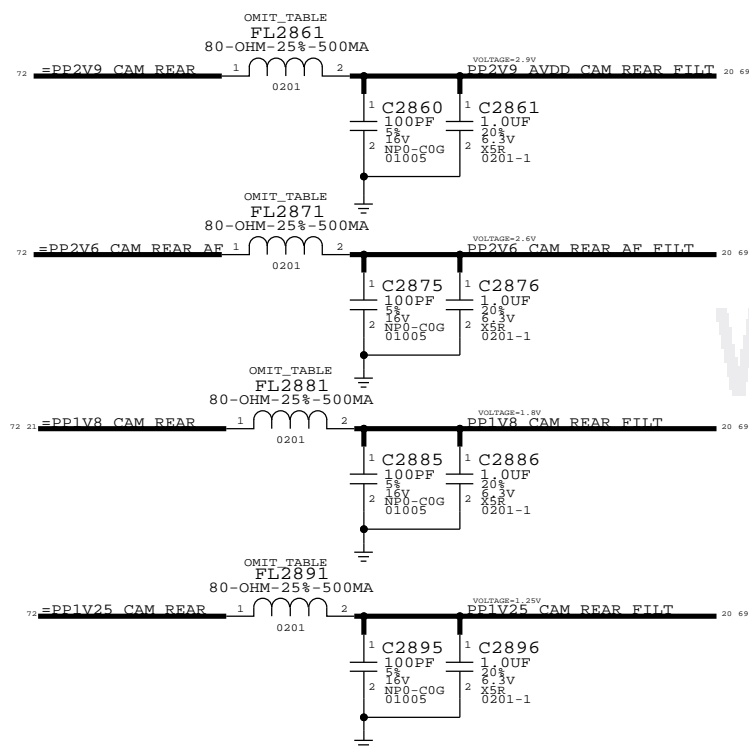
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# FRONT CAMERA SUPPORT

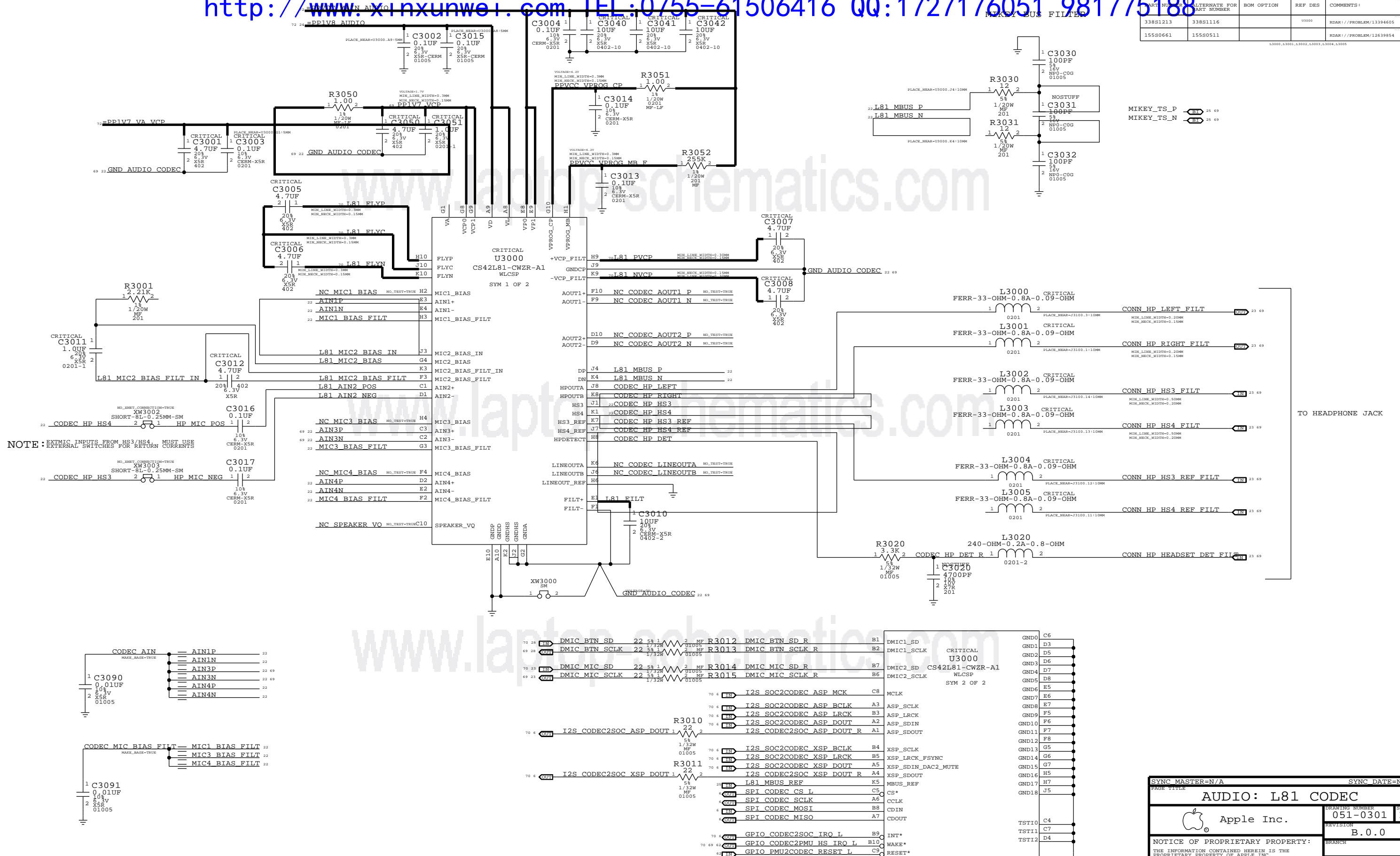


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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
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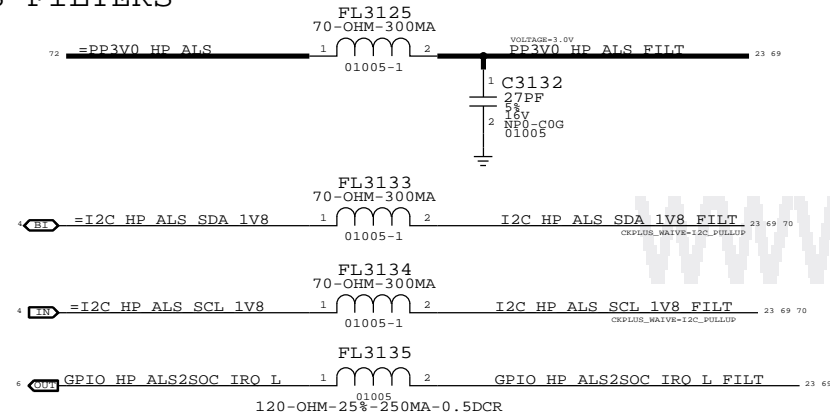


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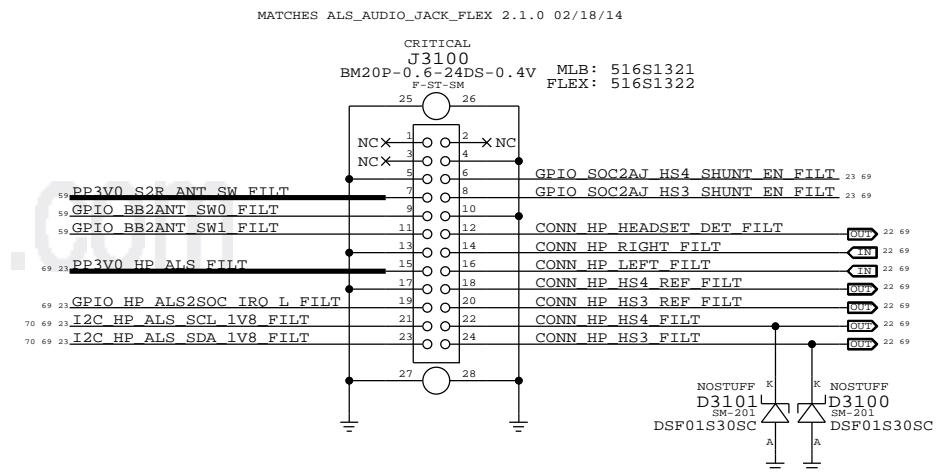
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# AUDIO JACK AND DMIC CONN

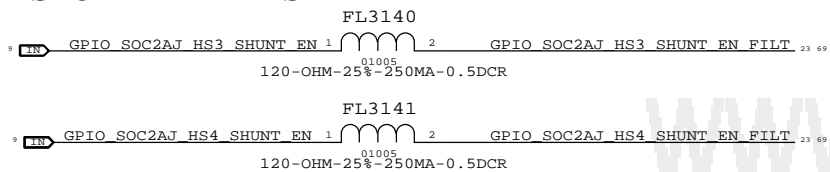
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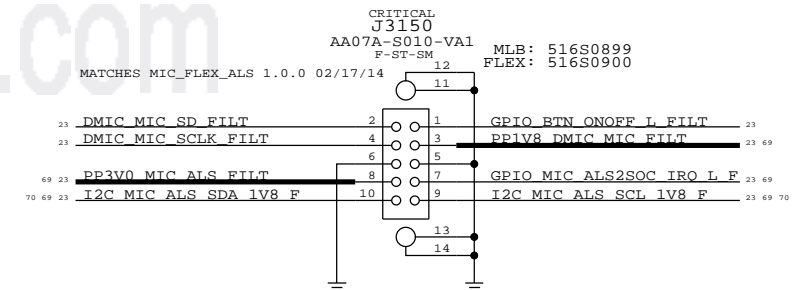
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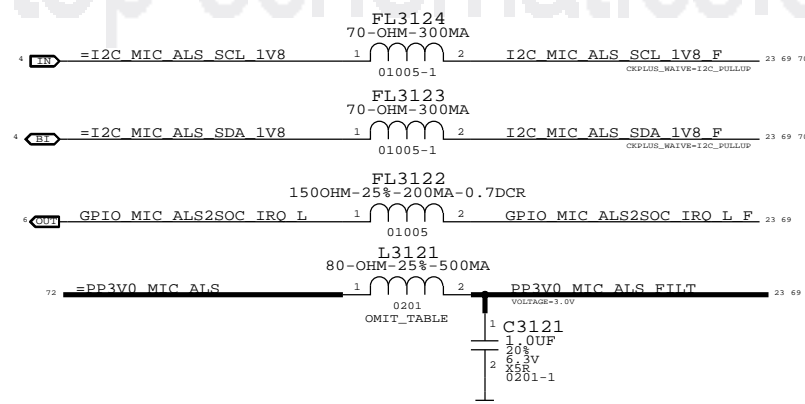
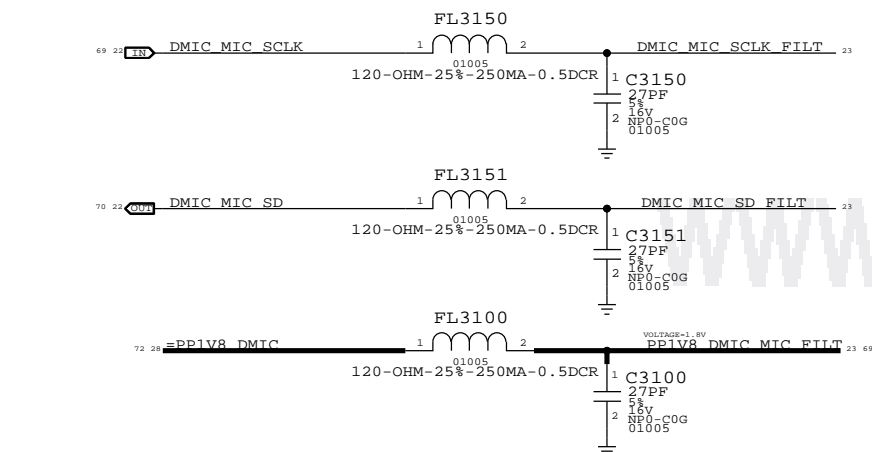
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## MIC FLEX CONNECTOR



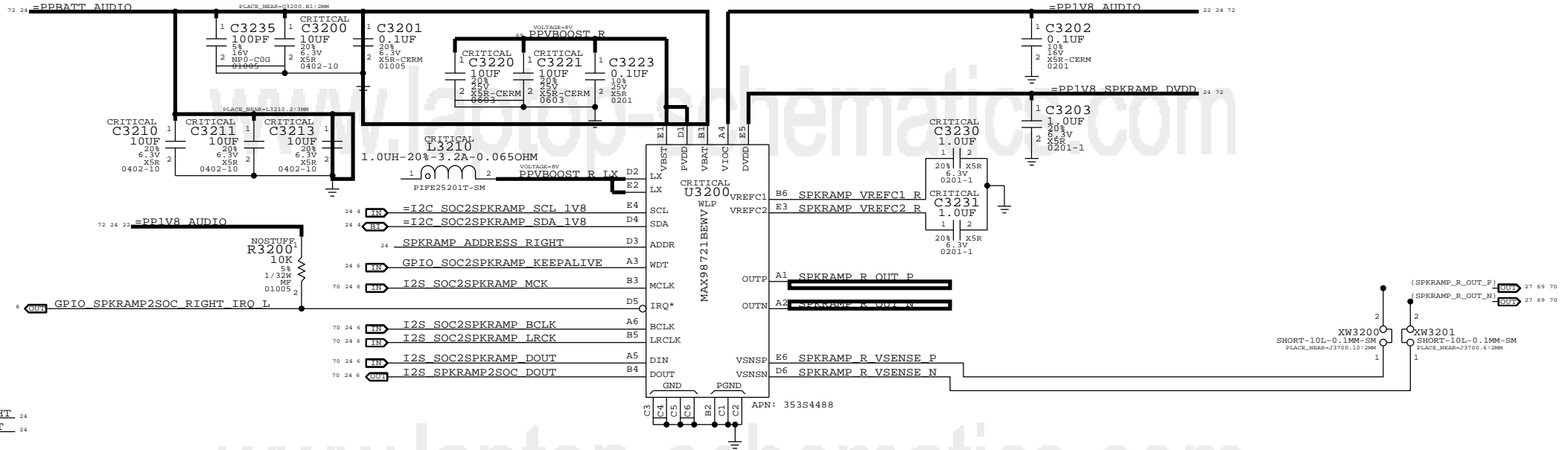
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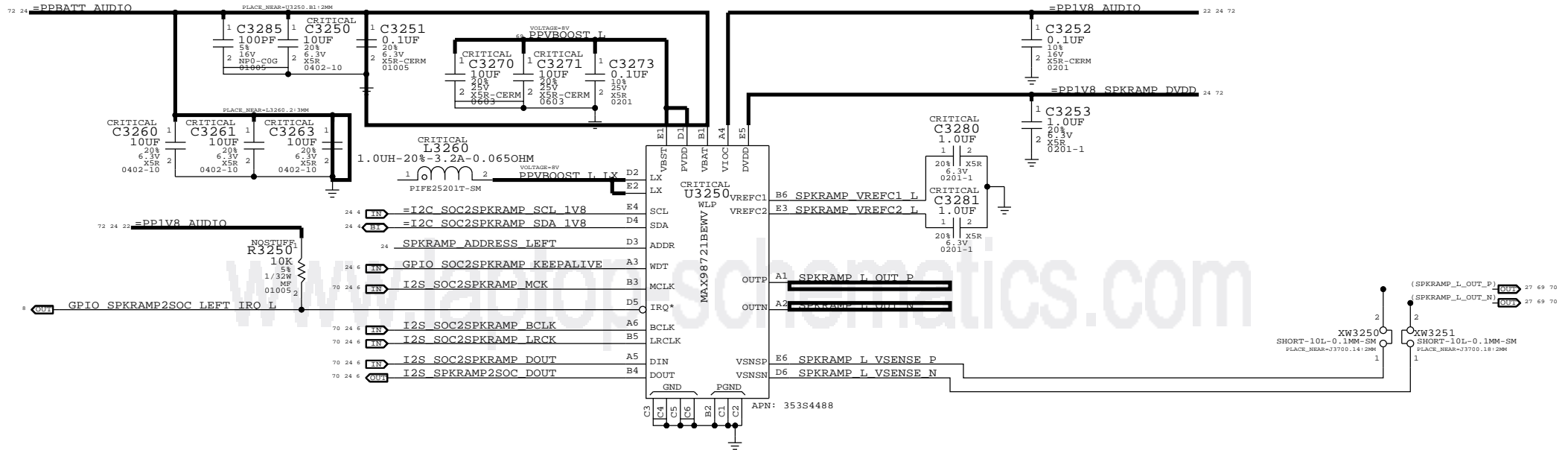
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PAGE TITLE		SYNC DATE=N/A	
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# RIGHT SPEAKER AMP



# LEFT SPEAKER AMP

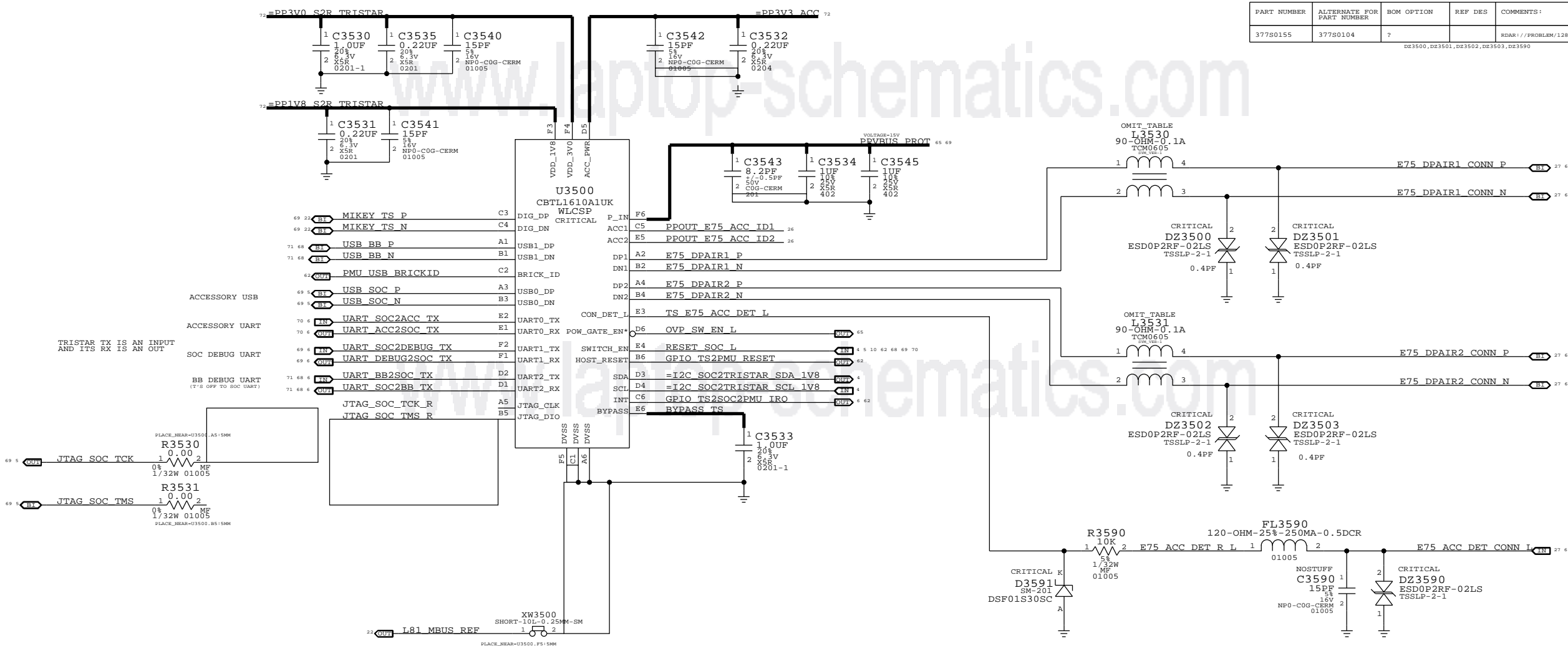



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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
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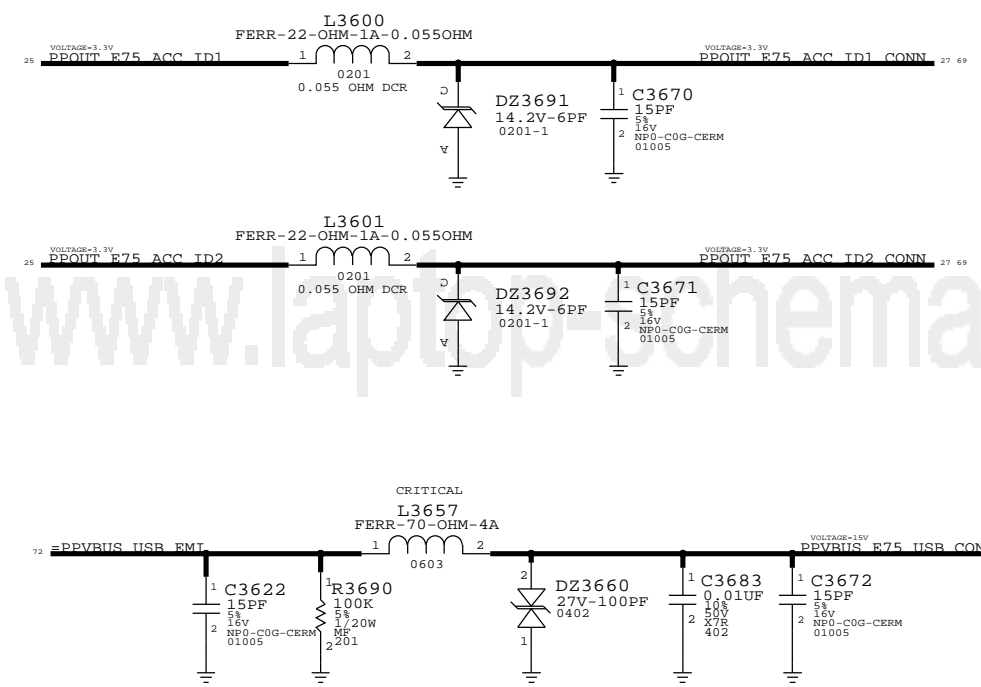
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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
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155S0741	155S0397		L3657	RDAR:///PROBLEM/11238851

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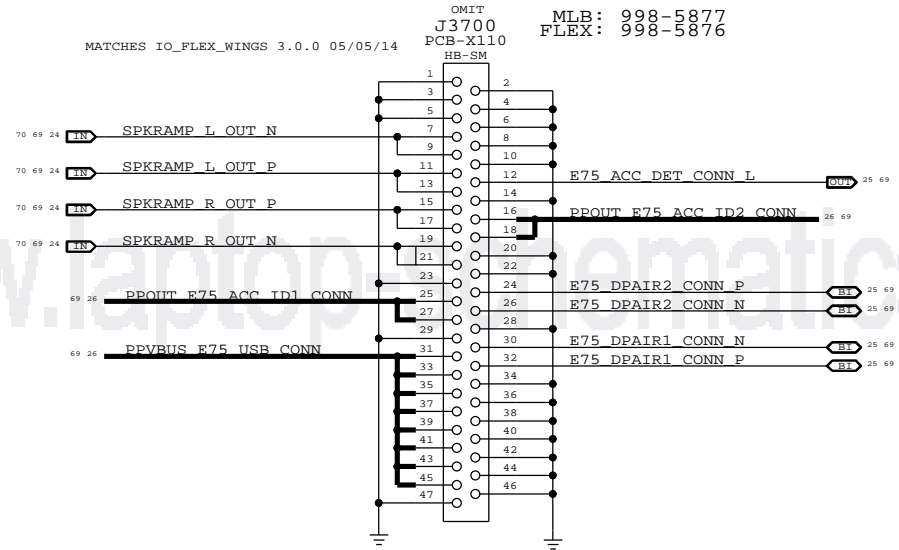
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IO FLEX HOTBAR PADS

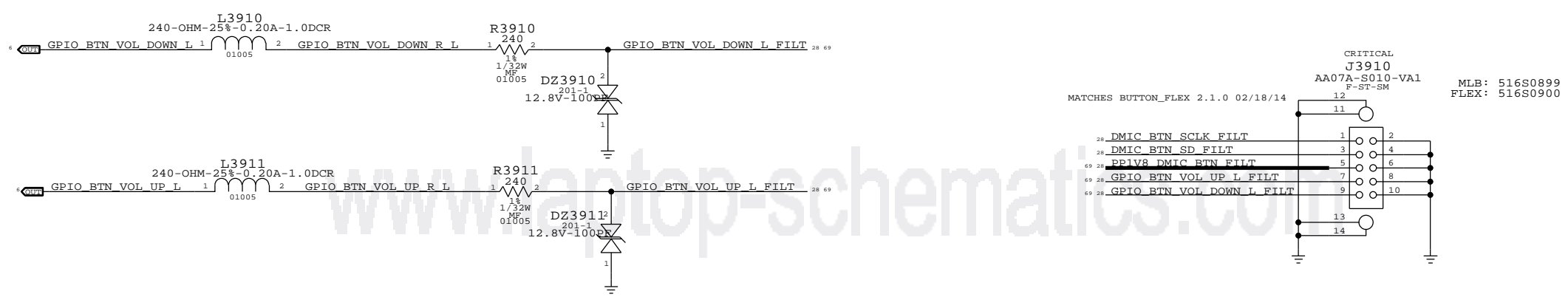


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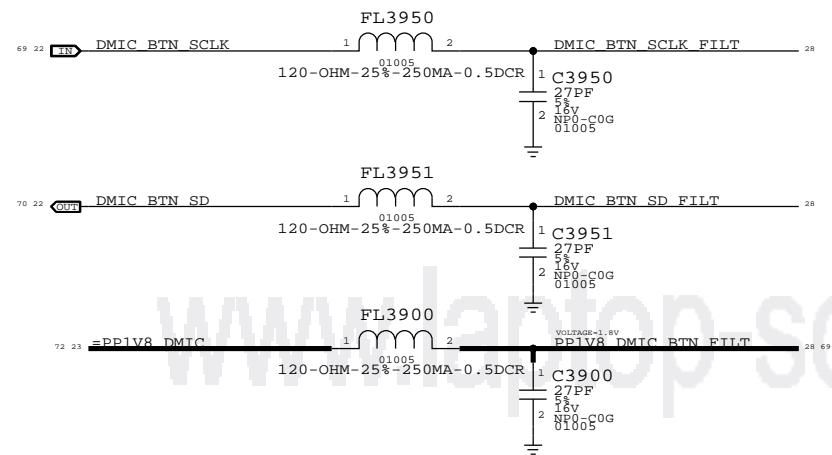
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BUTTON CONNECTOR



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STINGER

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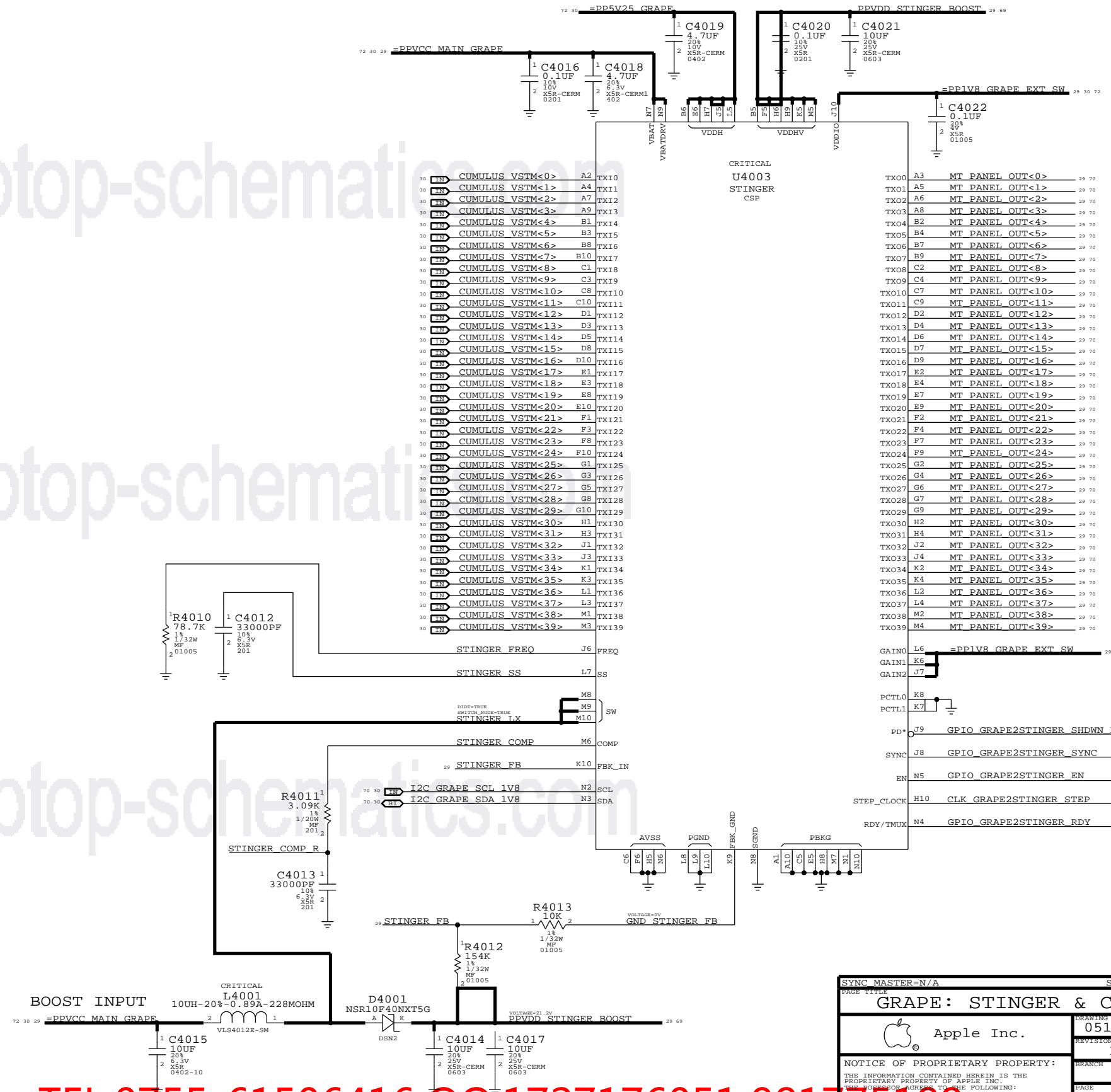
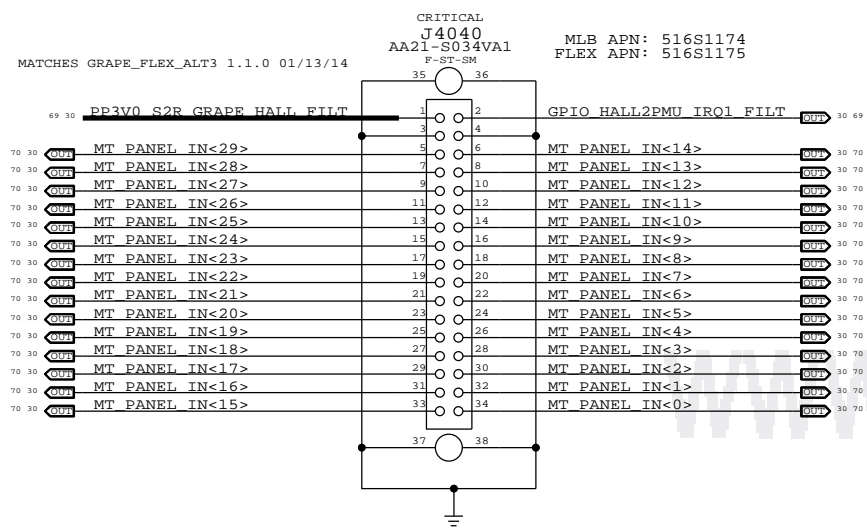
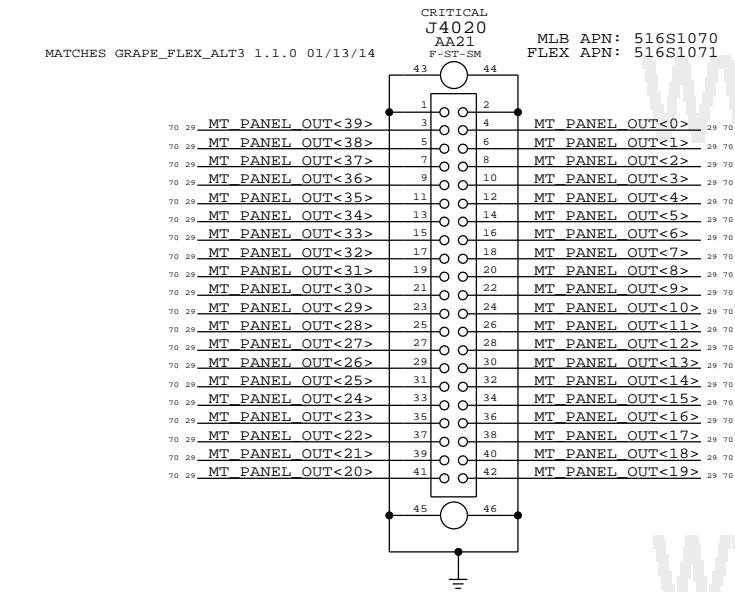
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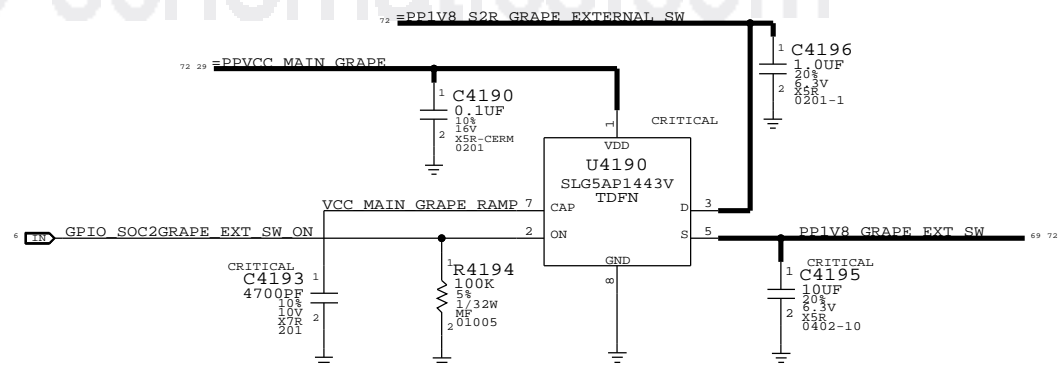
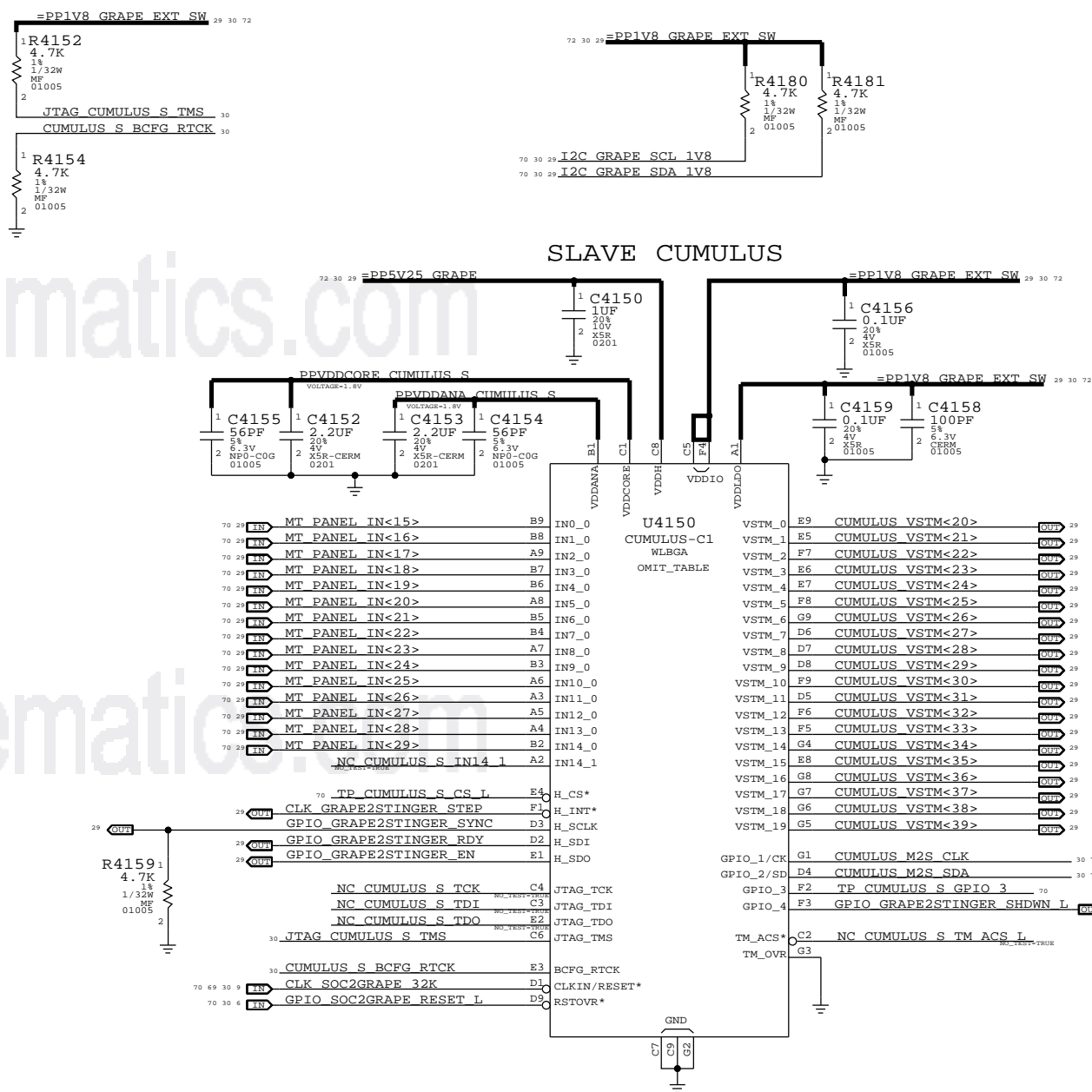
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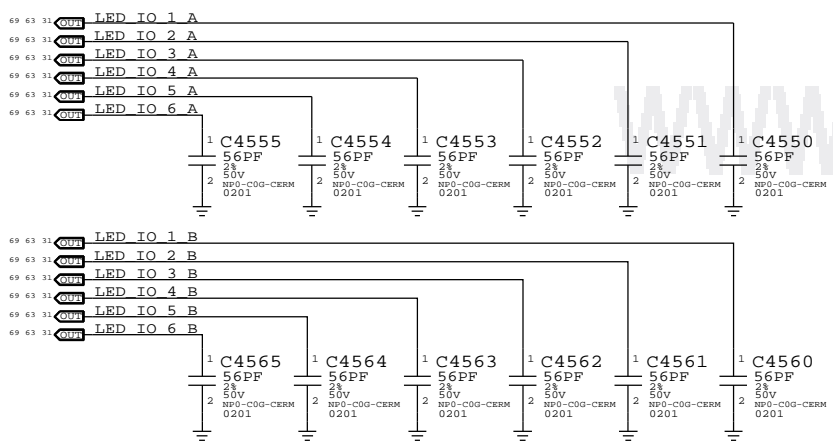
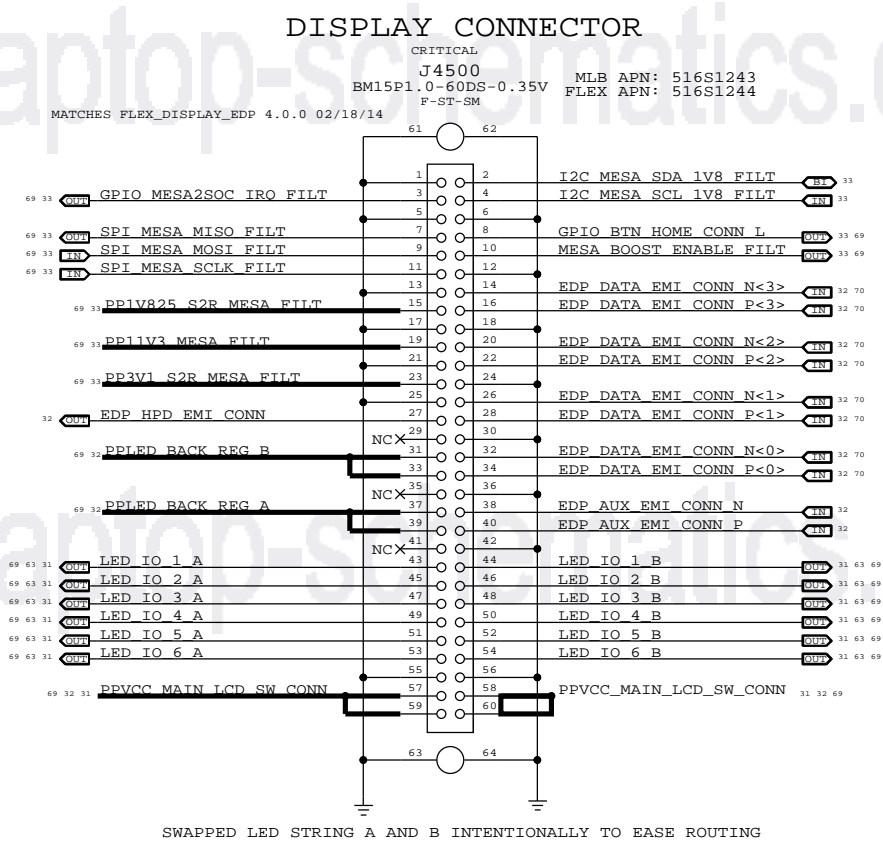
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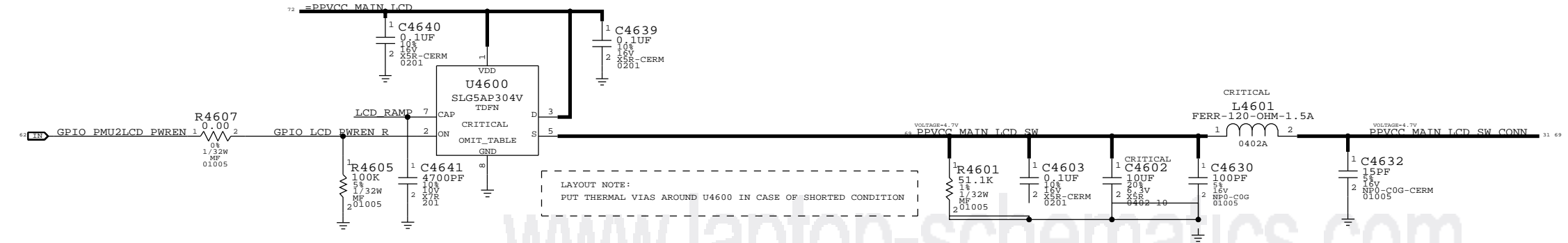
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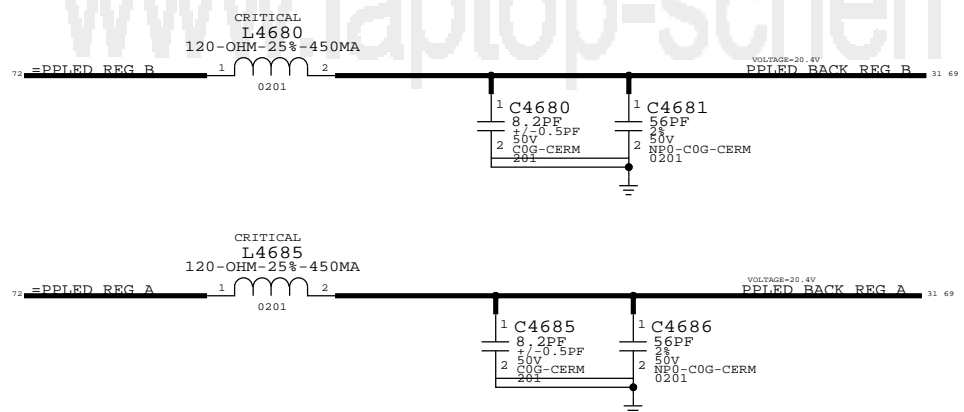
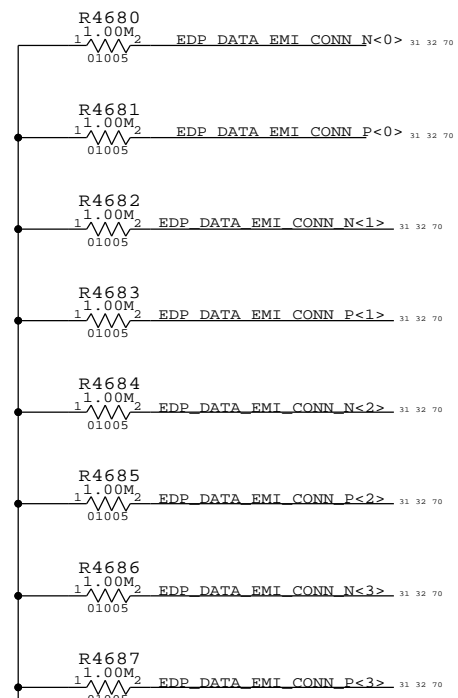
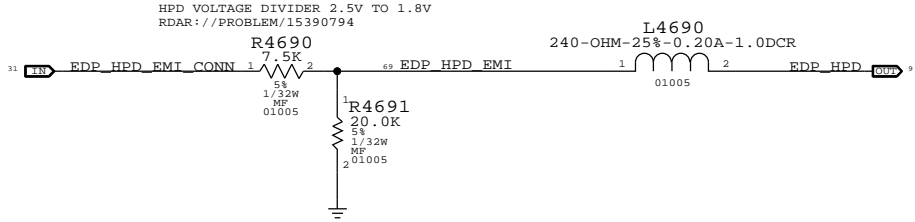
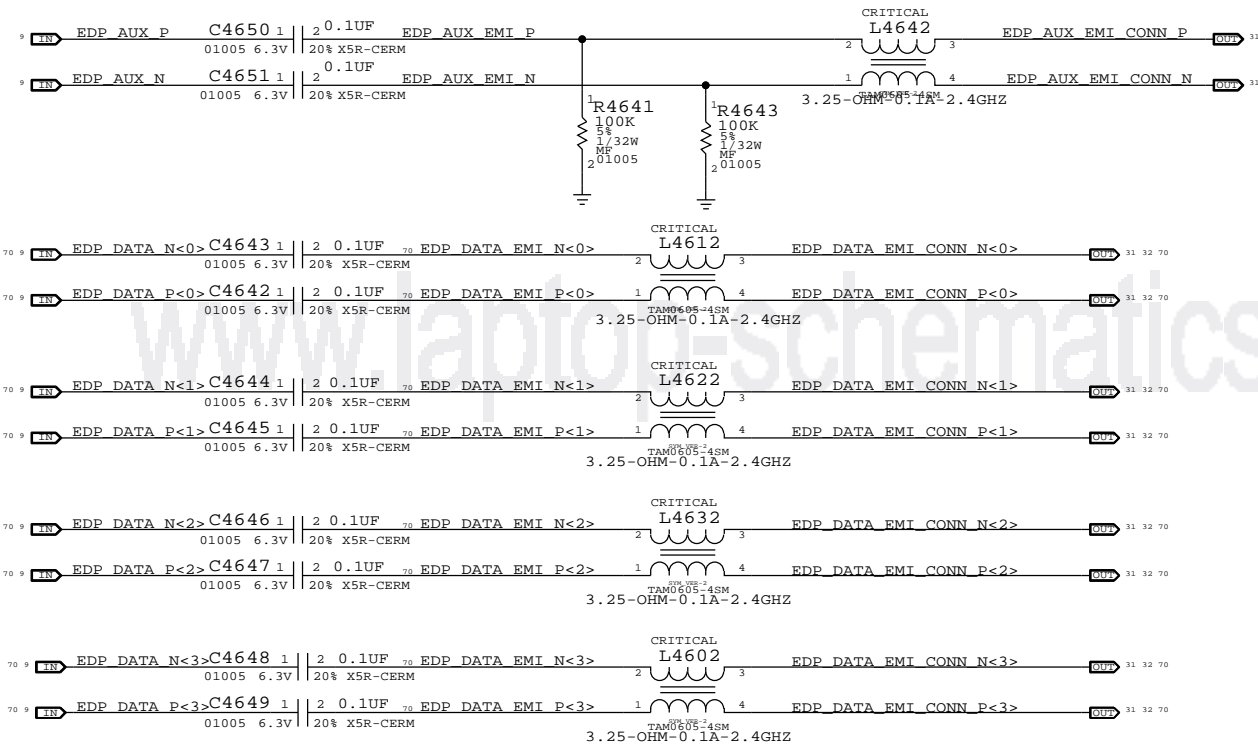


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155S0914	155S0897	?	L4602, ECT	RDAR://PROBLEM/15954071



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S4272	1	IC,SLG5AP1423V	U4600	CRITICAL	?



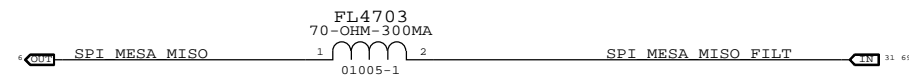
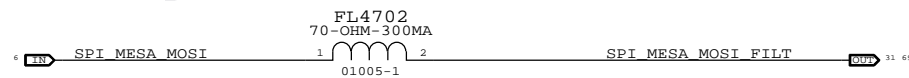
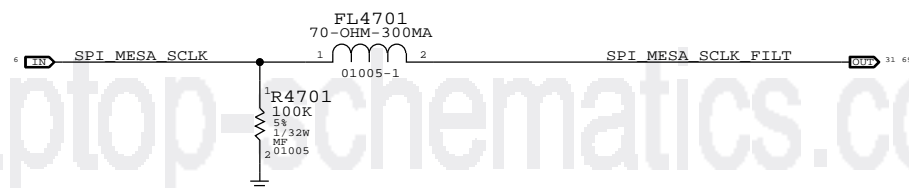
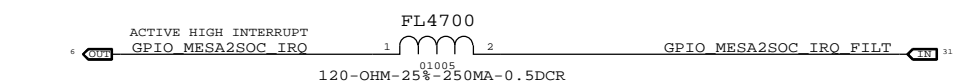
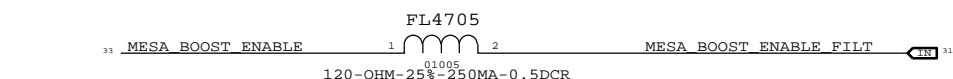
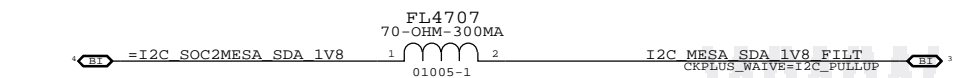
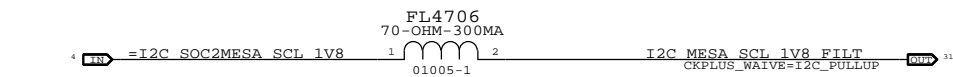
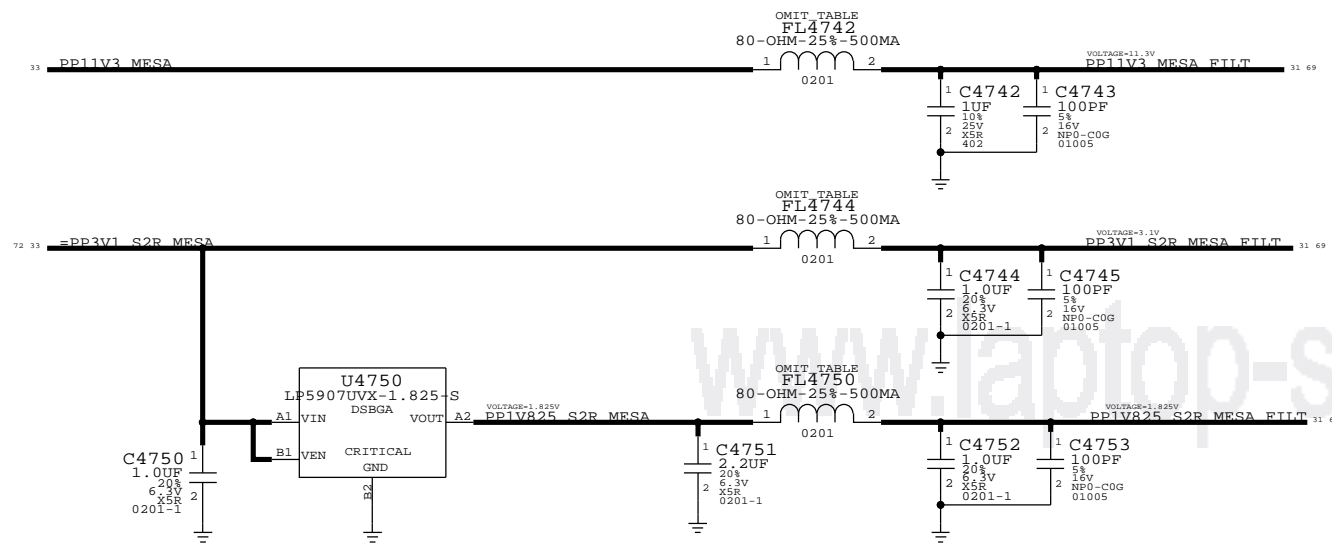
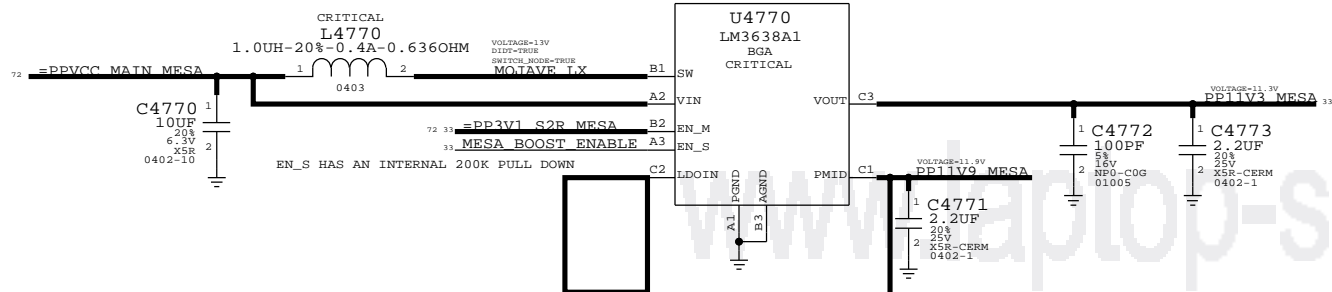
SYNC MASTER=N/A		SYNC DATE=N/A	
DISPLAY: EDP SUPPORT			
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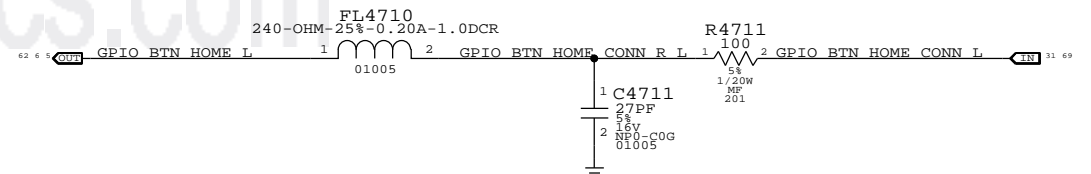
# MESA & HOME BUTTON

## MOJAVE

USING A1 BECAUSE NAVAJO NEEDS 11V3




## HOME BUTTON FILTERS



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S00017	155S0755			RDAR://PROBLEM/15807137

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S00018	155S0664			RDAR://PROBLEM/15796569

SYNC MASTER=N/A		SYNC DATE=N/A	
PAGE TITLE			
MESA: SUPPORT			
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		47 OF 155	
		SHEET	
		33 OF 73	

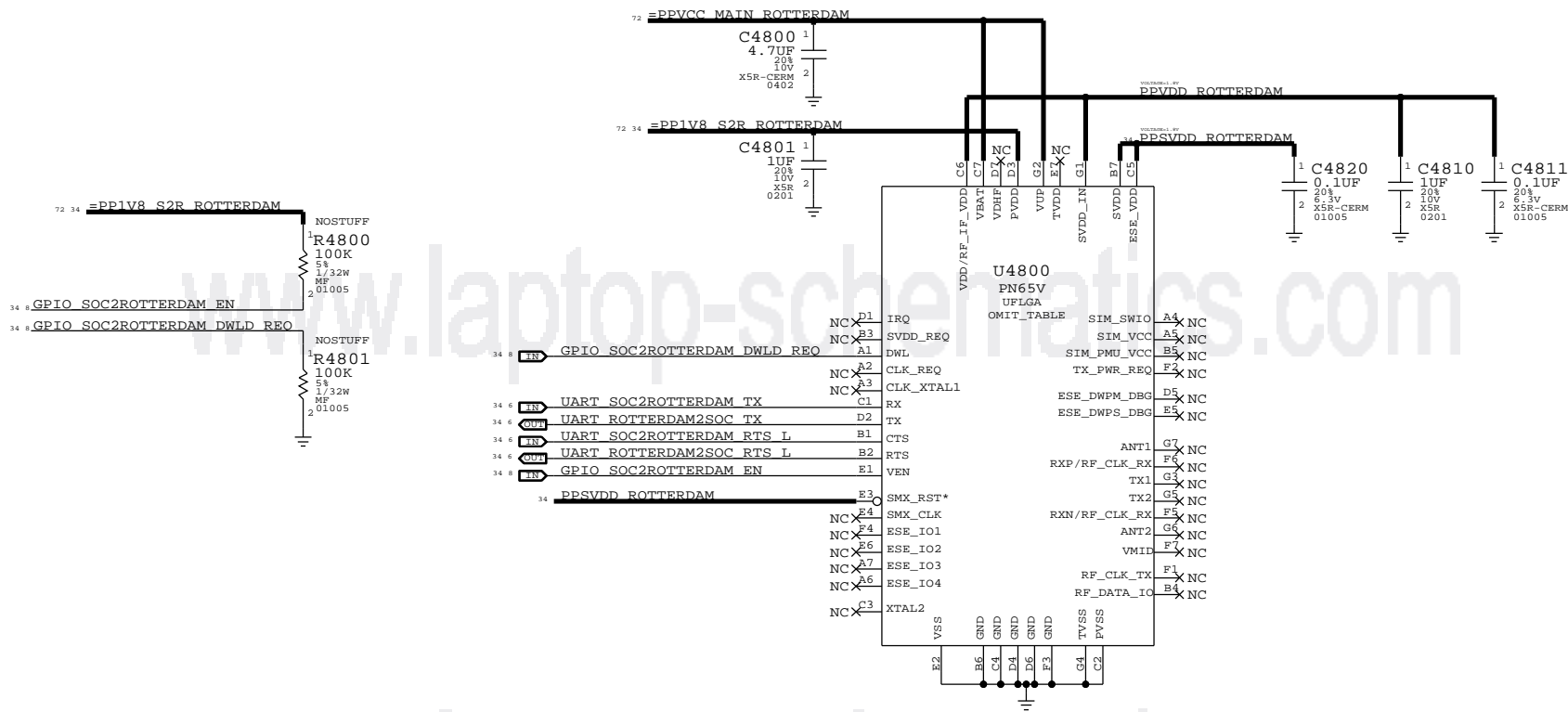
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J82

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ROTTERDAM

www.laptop-schematics.com



PP4800	0.5M	1	UART_SOC2ROTTERDAM_TX	6	34
PP4801	1.5M	1	UART_ROTTERDAM2SOC_TX	6	34
PP4802	2.5M	1	UART_SOC2ROTTERDAM_RTS_L	6	34
PP4803	3.5M	1	UART_ROTTERDAM2SOC_RTS_L	6	34
PP4804	4.5M	1	GPIO_SOC2ROTTERDAM_EN	8	34
PP4805	5.5M	1	GPIO_SOC2ROTTERDAM_DWLD_REQ	8	34

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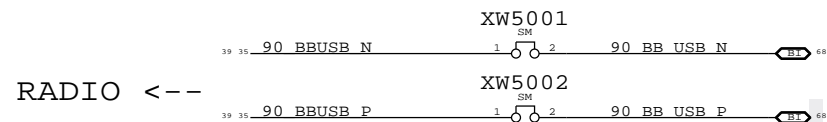
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SHEET	
34 OF 73	

# AP INTERFACE & DEBUG CONNECTOR

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## TEST POINTS

TP5000 A 1 50_BB_HSIC_STROBE TP-PS	39 68	TP5009 A 1 BB_JTAG_RST_L TP-PS	35 39
TP5001 A 1 50_BB_HSIC_DATA TP-PS	39 68	TP5010 A 1 BB_JTAG_TCK TP-PS	35 39
TP5002 A 1 BB_DEBUG_ERROR TP-PS	40	TP5011 A 1 BB_JTAG_TMS TP-PS	35 39
TP5003 A 1 PS_HOLD_PMIC TP-PS	35 37	TP5012 A 1 BB_JTAG_TDO TP-PS	35 39
TP5004 A 1 PMIC_RESOUT_L TP-PS	35 37 39	TP5013 A 1 BB_JTAG_TDI TP-PS	35 39
TP5005 A 1 MDM_CLK TP-PS	37 39	TP5014 A 1 BB_JTAG_TRST_L TP-PS	35 39
TP5006 A 1 PP_LD011 TP-PS	35 36 38 39 40 42	TP5015 A 1 BB_DEBUG_STATUS TP-PS	40
TP5007 A 1 SPMI_DATA TP-PS	37 39	TP5016 A 1 BOOT_HSIC TP-PS	35 40
TP5008 A 1 SPMI_CLK TP-PS	37 39	TP5017 A 1 RFFE1_CLK TP-PS	35 40 44 45 46 47 48 49
TP5025 A 1 BOUNDARY_SCAN_EN TP-PS	39 69	TP5018 A 1 RFFE1_DATA TP-PS	35 40 44 45 46 47 48 49
TP5021 A 1 PP_BATT_VCC TP-PS	35 44 53 68 73	TP5019 A 1 RFFE2_CLK TP-PS	35 40 50 51 53
TP5028 A 1 TP-PS		TP5020 A 1 RFFE2_DATA TP-PS	35 40 50 51 53
TP5026 A 1 TP-PS		TP5031 A 1 90_BBUSB_N TP-PS	35 39
TP5027 A 1 TP-PS		TP5030 A 1 90_BBUSB_P TP-PS	35 39



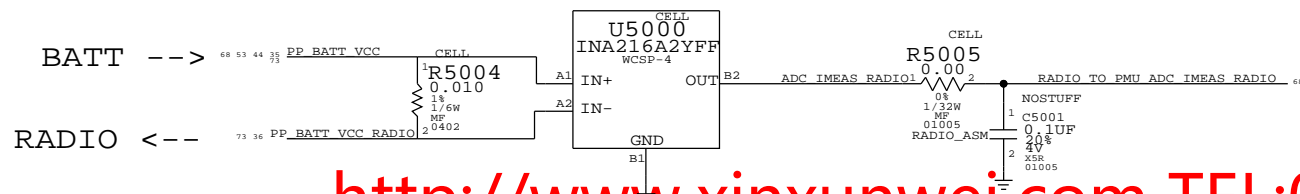
## PROBE POINTS

PP5000 P 1 SLEEP_CLK_32K PP	37 39
PP5001 P 1 BB_EEPROM_SCL PP	39 40
PP5002 P 1 BB_EEPROM_SDA PP	39 40
PP5003 P 1 ET_DAC_P PP	40 44
PP5004 P 1 ET_DAC_N PP	40 44
TP5029 A 1 PP_LD06 TP-PS	36 69 71 73

## CONFIG\_RF BOM OPTIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
131S0273	1	0.8PF 0201	C6001	CRITICAL	X137_RF
131S0273	1	0.8PF 0201	C6001	CRITICAL	X202_RF
131S0431	1	0.2PF 0201	C6013	CRITICAL	X190_RF
131S0273	1	0.8PF 0201	C6013	CRITICAL	X137_RF
131S0273	1	0.8PF 0201	C6013	CRITICAL	X202_RF
152S2020	1	3.6NH +/-0.1NH 400MA 0201	L6001	CRITICAL	X190_RF
152S2022	1	4.3NH 3% 500MA 0201	L6001	CRITICAL	X137_RF
152S2022	1	4.3NH 3% 500MA 0201	L6001	CRITICAL	X202_RF
131S0323	1	1.1PF 0201	C6421	CRITICAL	X190_RF
152S1217	1	1.0NH +/-0.1NH 750MA 0201	L6402	CRITICAL	X190_RF
152S2042	1	1.8NH +/-0.1NH 800MA 0201	L6402	CRITICAL	X137_RF
152S2042	1	1.8NH +/-0.1NH 800MA 0201	L6402	CRITICAL	X202_RF
152S1994	1	6.8NH 3% 210MA 01005	C6202	CRITICAL	X190_RF
152S1977	1	10.0NH 3% 170MA 01005	C6202	CRITICAL	X137_RF
152S1994	1	6.8NH 3% 210MA 01005	C6202	CRITICAL	X202_RF
152S00028	1	22NH 3% 120MA 01005	L6720	CRITICAL	X190_RF
152S1979	1	18NH 1% 140MA 01005	L6720	CRITICAL	X137_RF
152S1979	1	18NH 1% 140MA 01005	L6720	CRITICAL	X202_RF
138S0831	5	MURATA 2.2UF CAPACITOR	C5101,C5121,C5122,C6010,C6011	CRITICAL	CELL

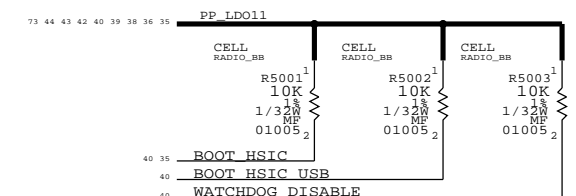
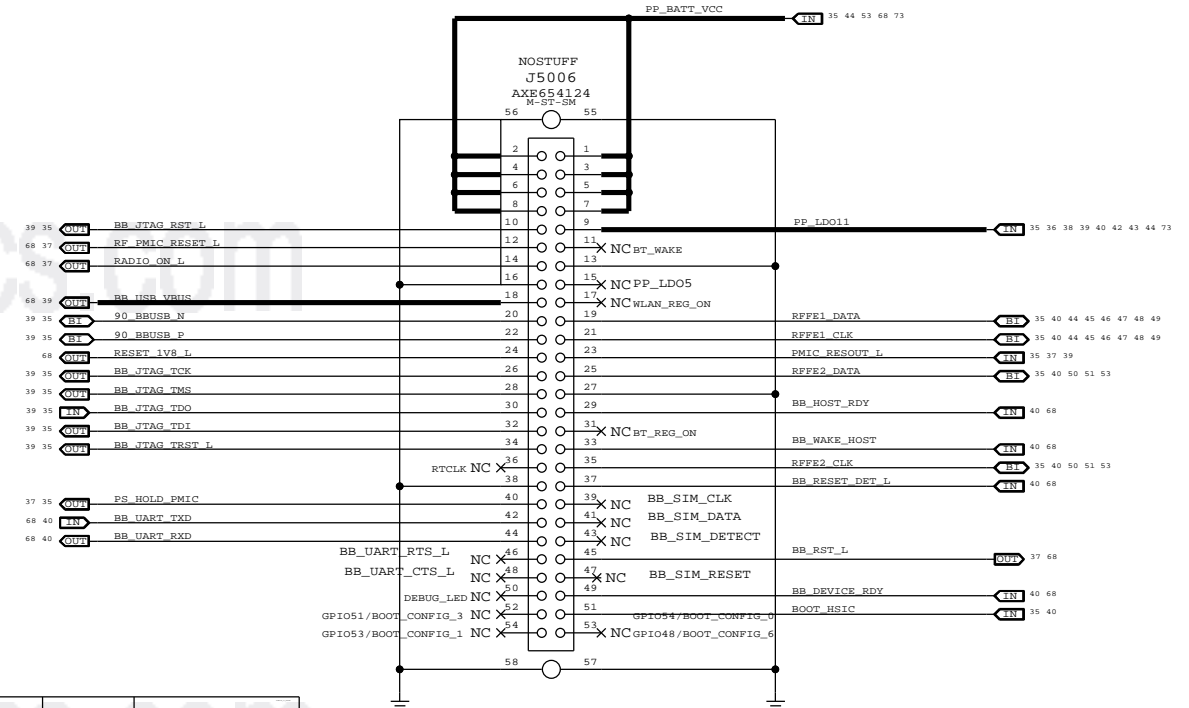
## PP\_VCC\_MAIN CURRENT SENSE




## BOM ALTERNATES

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152S1850	152S1721		L5001,L5103,L5104	MURATA IN, 2.2UF, 2016
152S2050	152S1857		L5902	TAIYO IND, 2.2UF, 2012

## DEBUG CONNECTOR



REVISION DATE: 9/29/2014

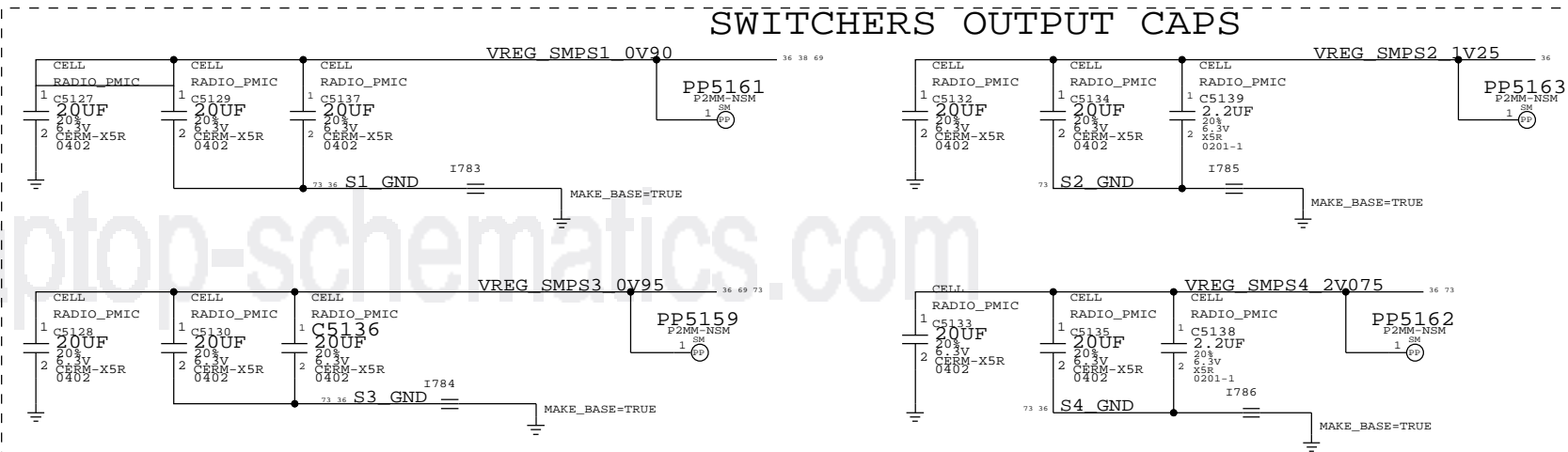
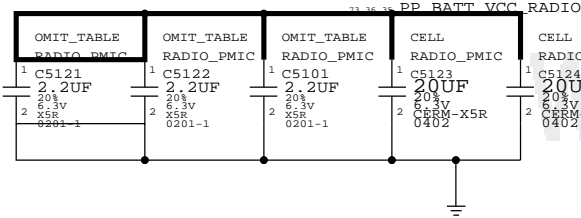
SYNC MASTER=RADIO		SYNC DATE=09/29/2014	
PAGE 50 OF 155			
CELL: PROBE PTS & DEBUG CONN			
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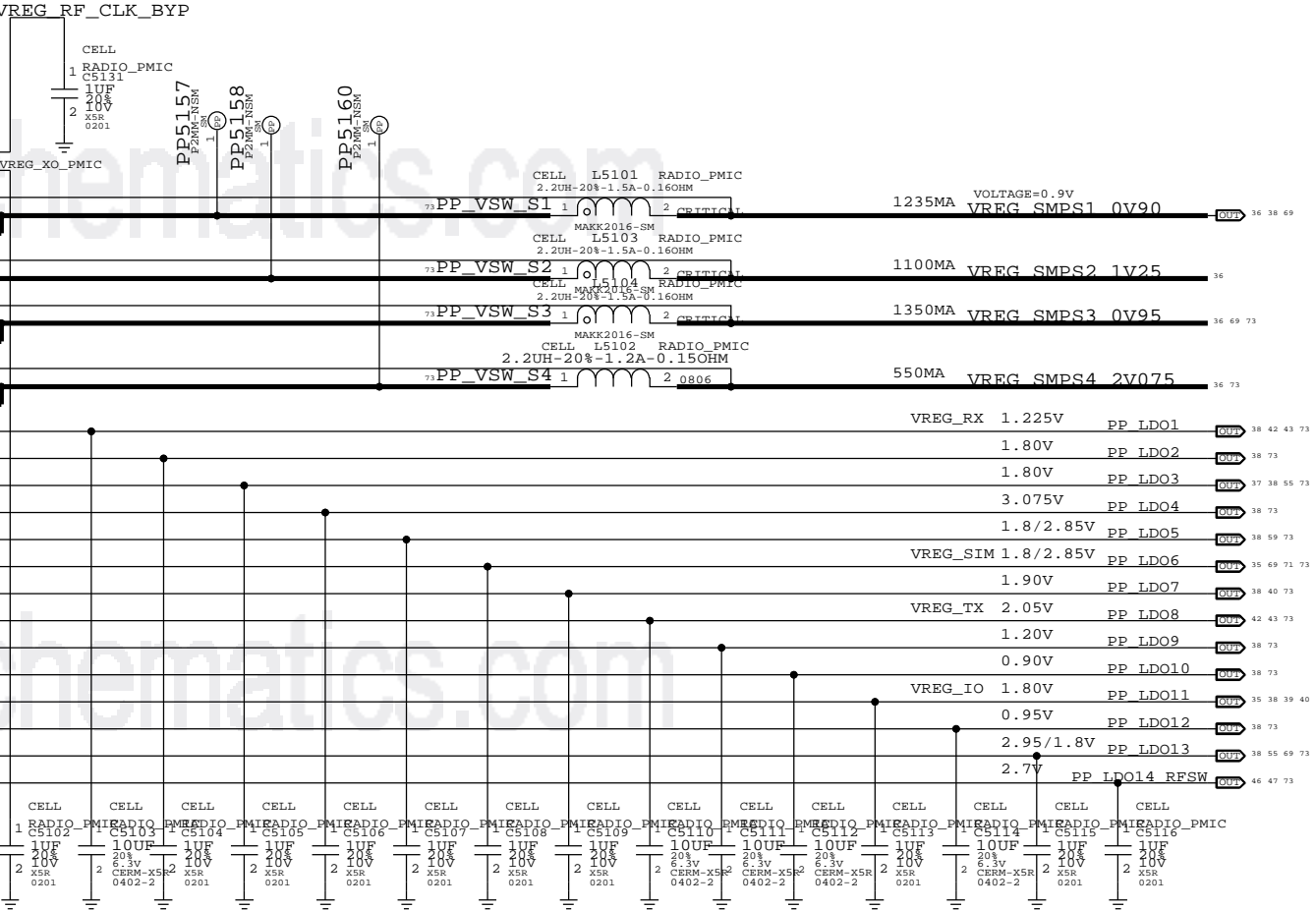
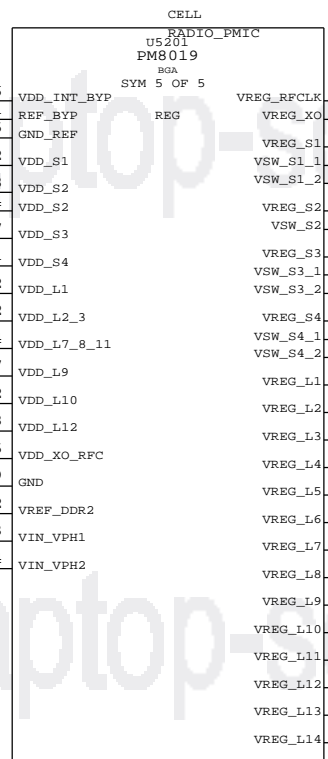
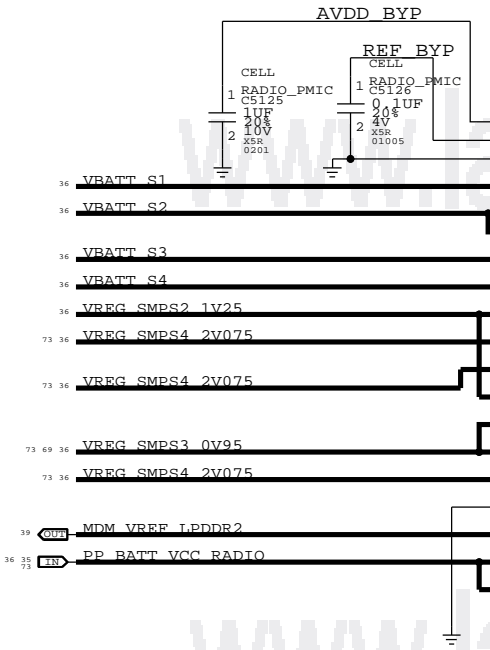
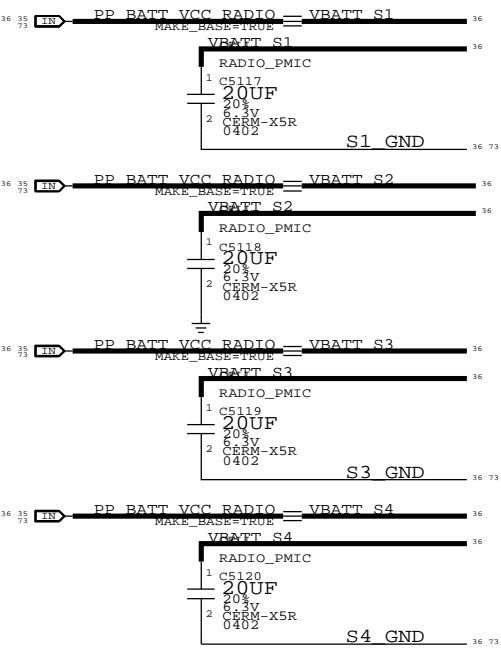
# BASEBAND PMU (1 OF 2)


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C332  
R302  
L304  
U301



## SWITCHERS BULK CAPS

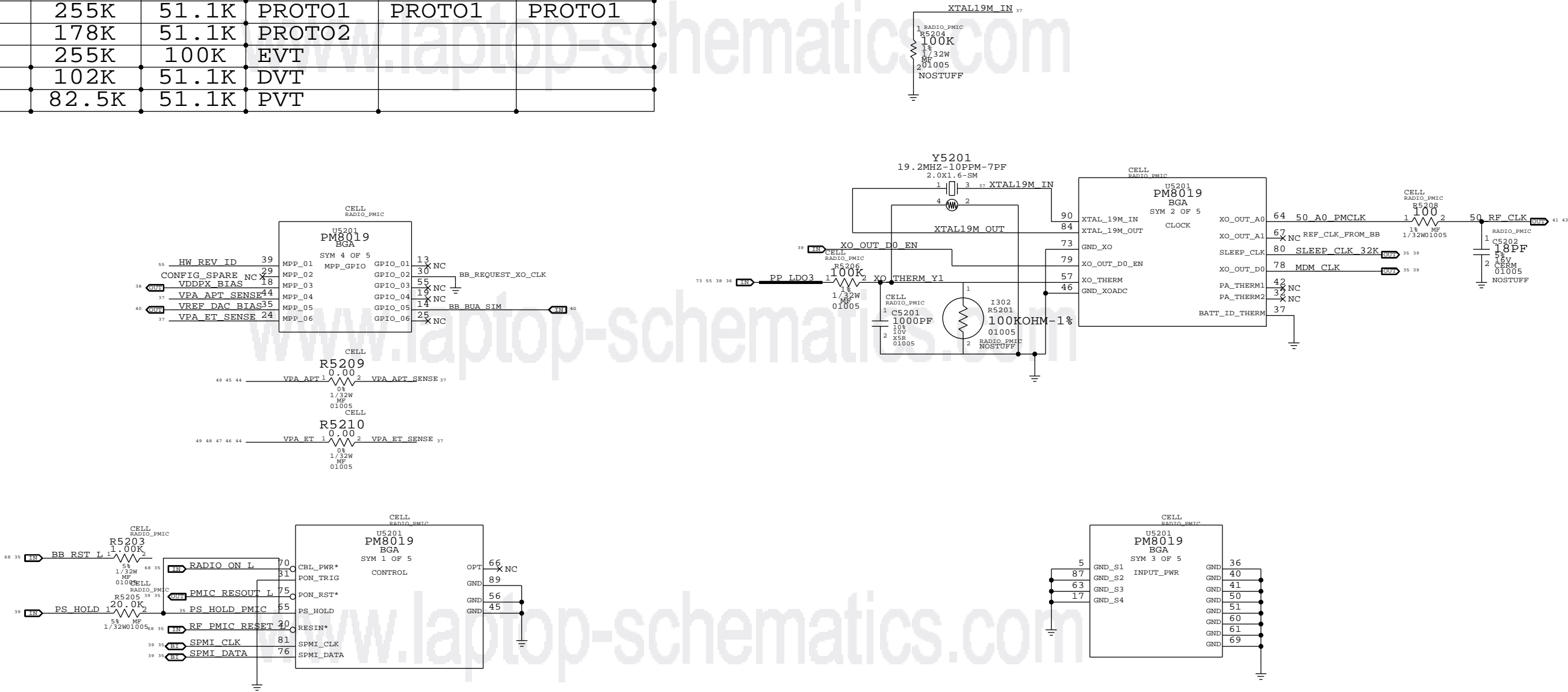


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	Revision	B.0.0
	Branch	
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C401
R411
L400
U404

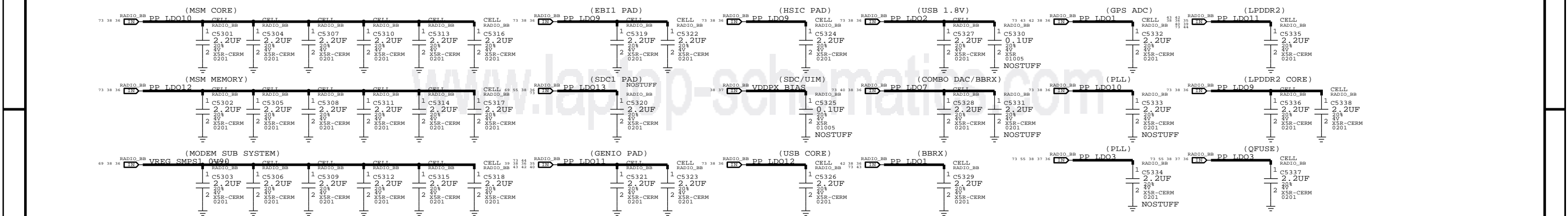
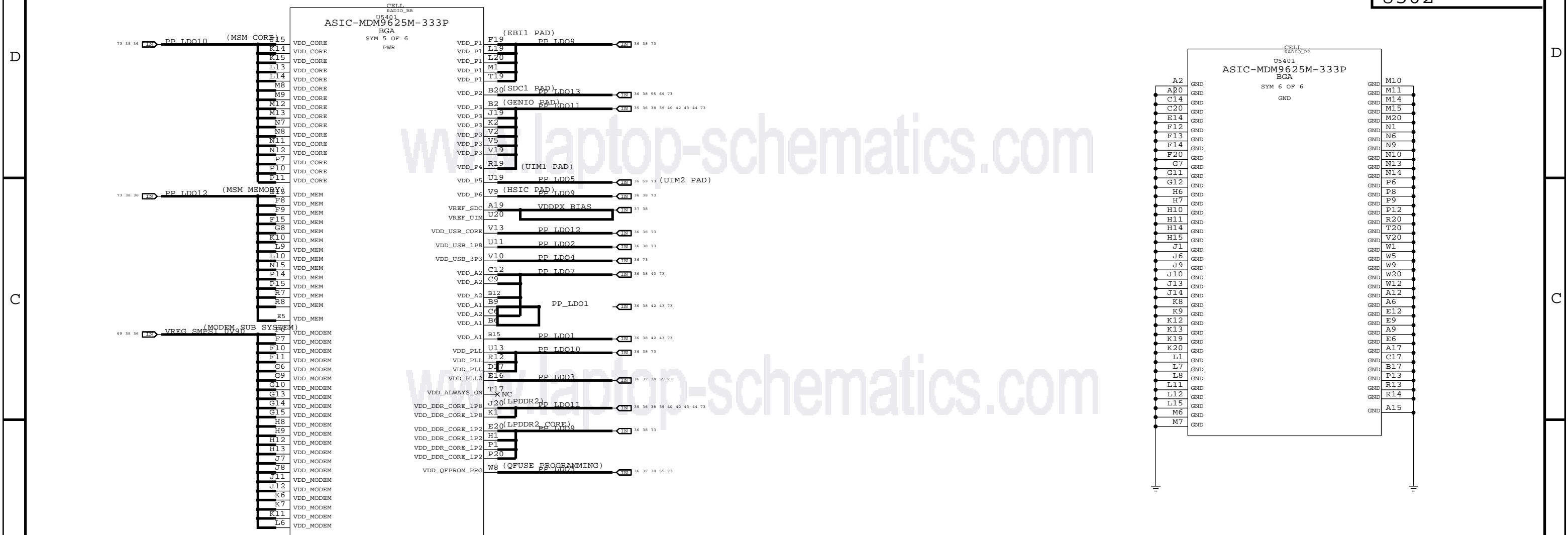
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0.20V	422K	51.1K	PROTO0	PROTO0B	PROTO0
0.30V	255K	51.1K	PROTO1	PROTO1	PROTO1
0.40V	178K	51.1K	PROTO2		
0.50V	255K	100K	EVT		
0.60V	102K	51.1K	DVT		
0.70V	82.5K	51.1K	PVT		





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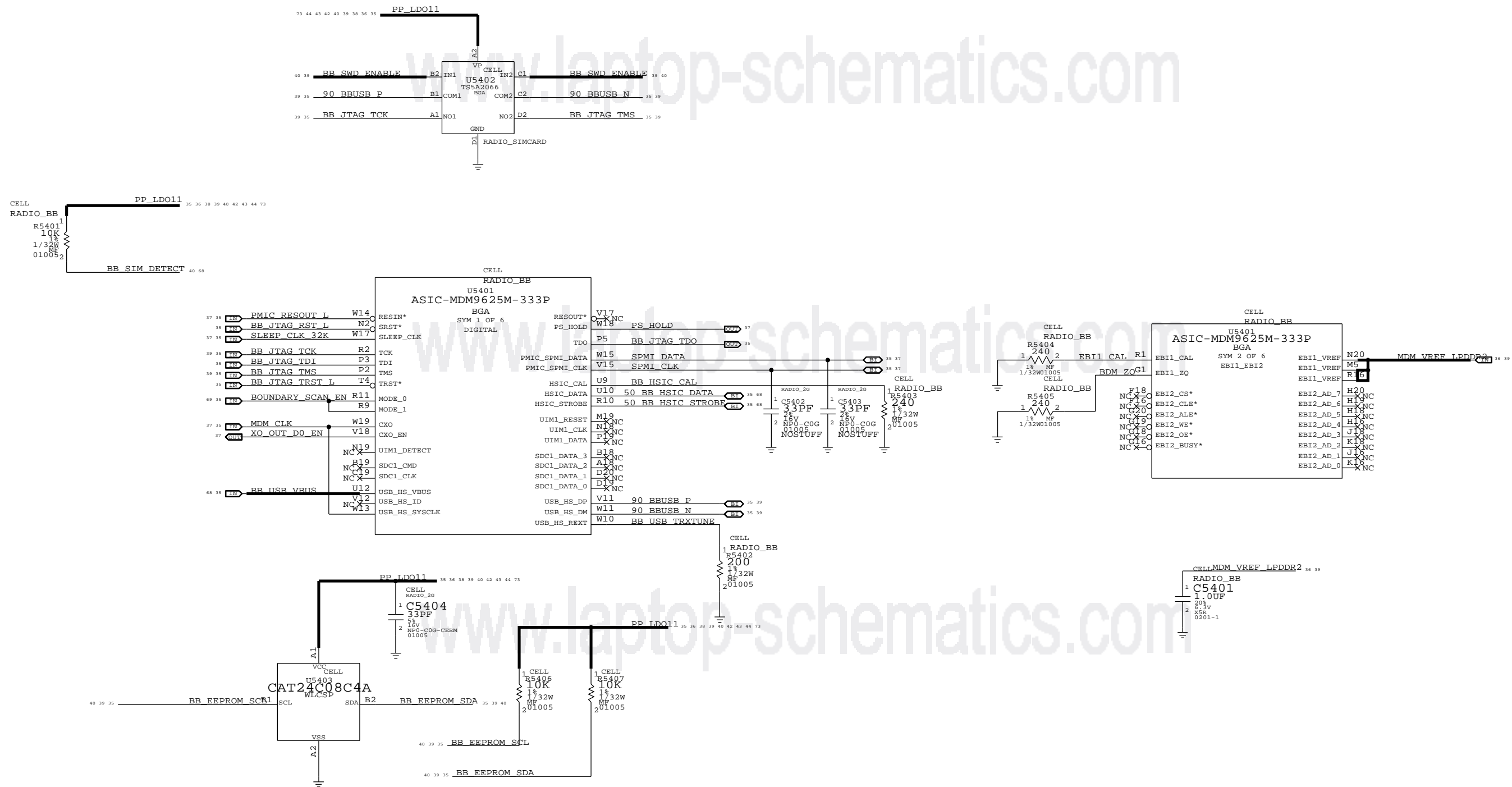
C538
R500
L500
U502



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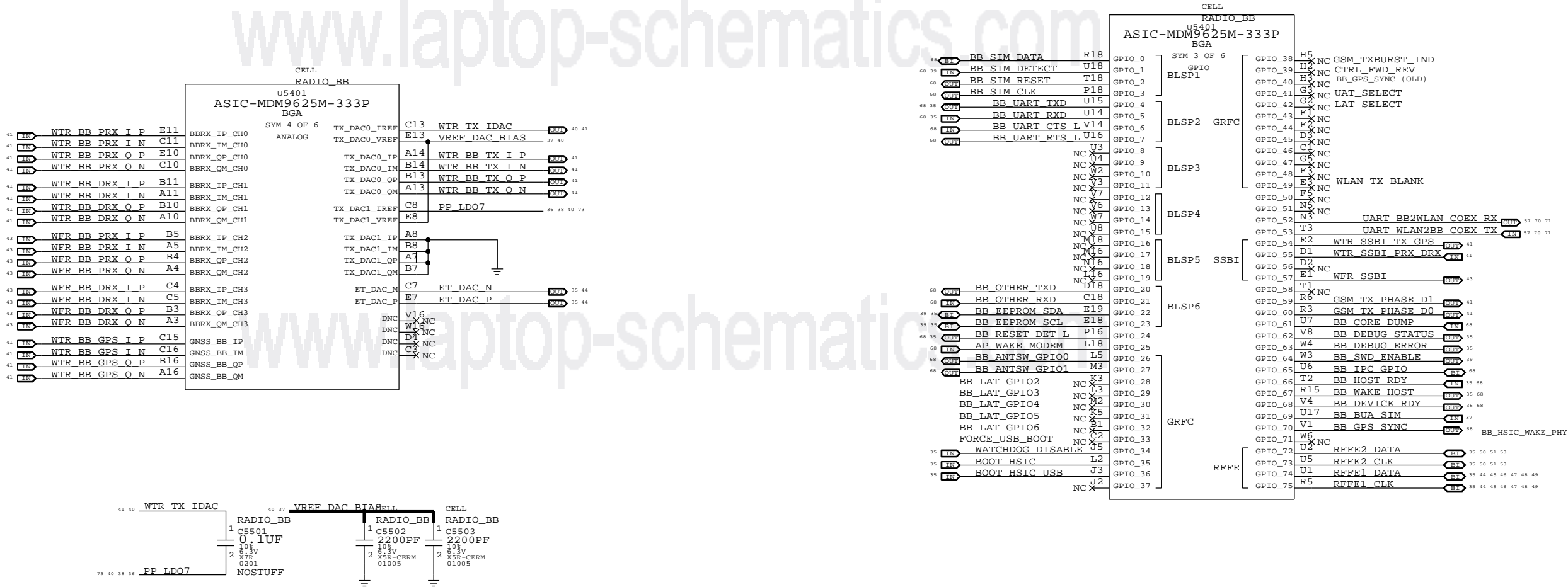
C600
R606
L600
U602



BASEBAND (3 OF 3)

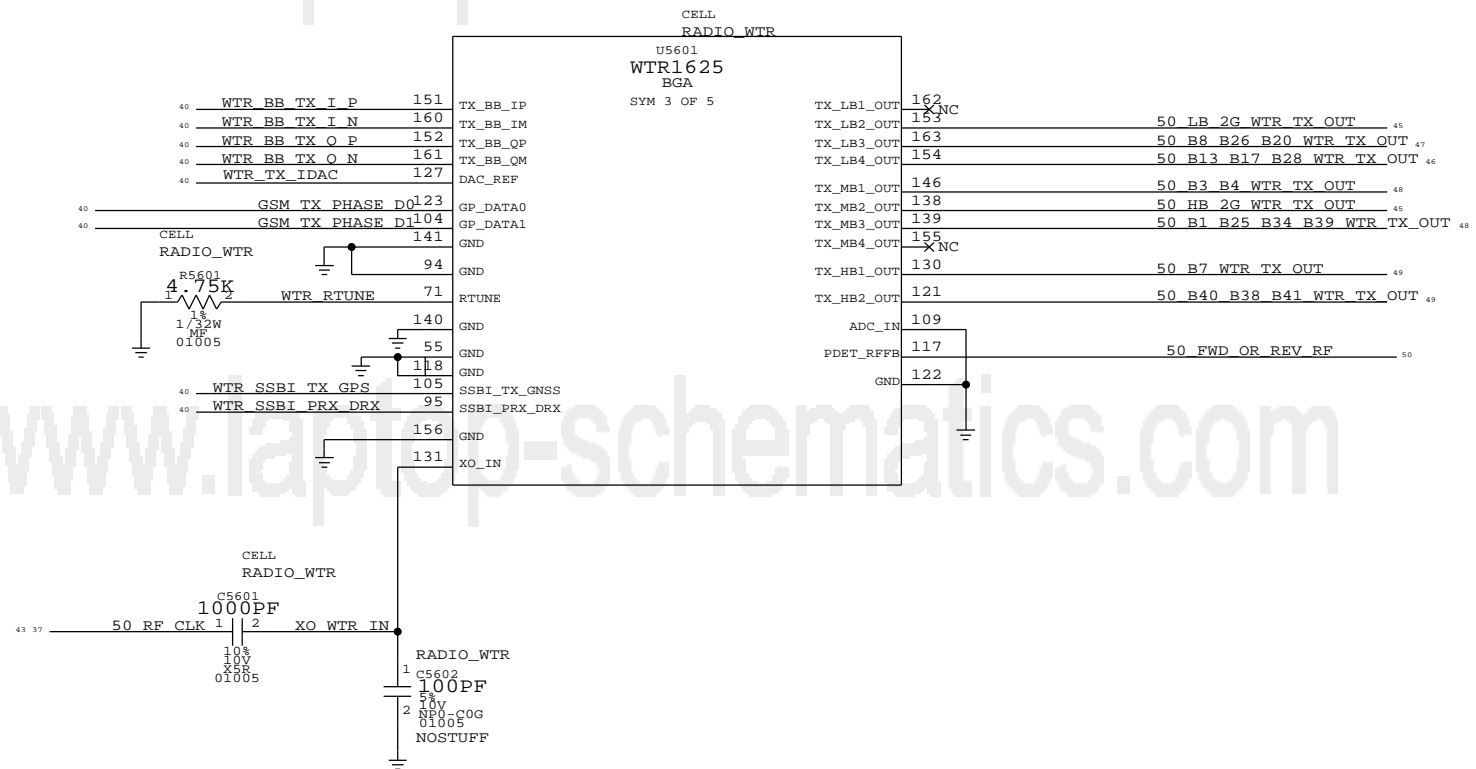
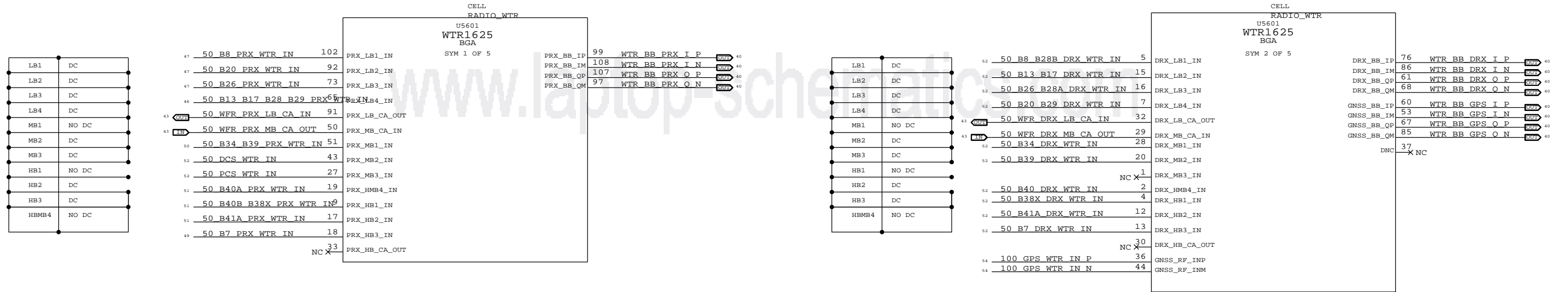
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C704  
R700  
L700  
U702




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C802
R802
L800
U803



RF\_CLK IS SHARED BETWEEN WTR AND WFR. LENGTH DIFFERENCE BETWEEN THE TWO SHOULD BE < 5MM.

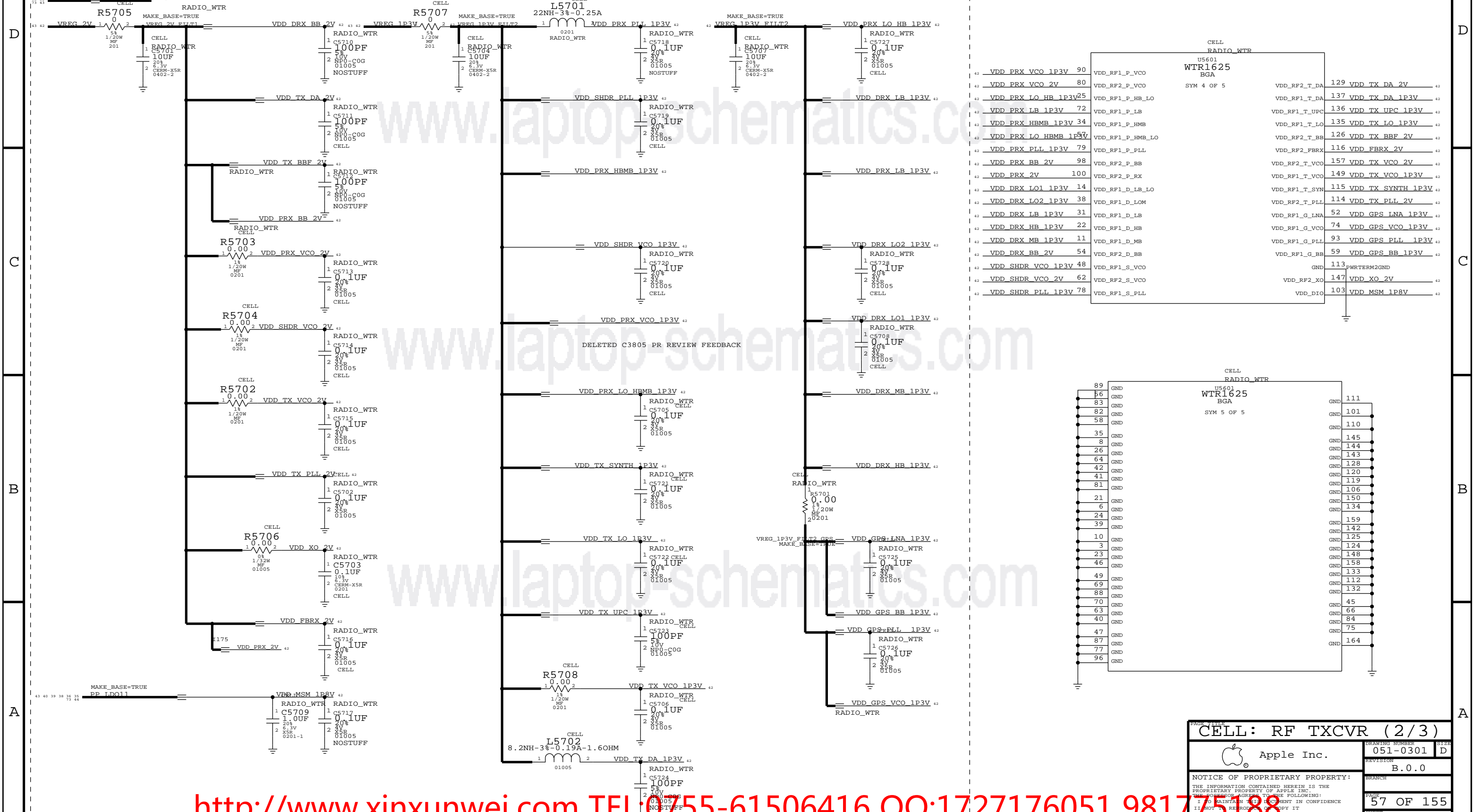
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C934
R926
L3802_RF
U902

## WTR DECOUPLING CAPS



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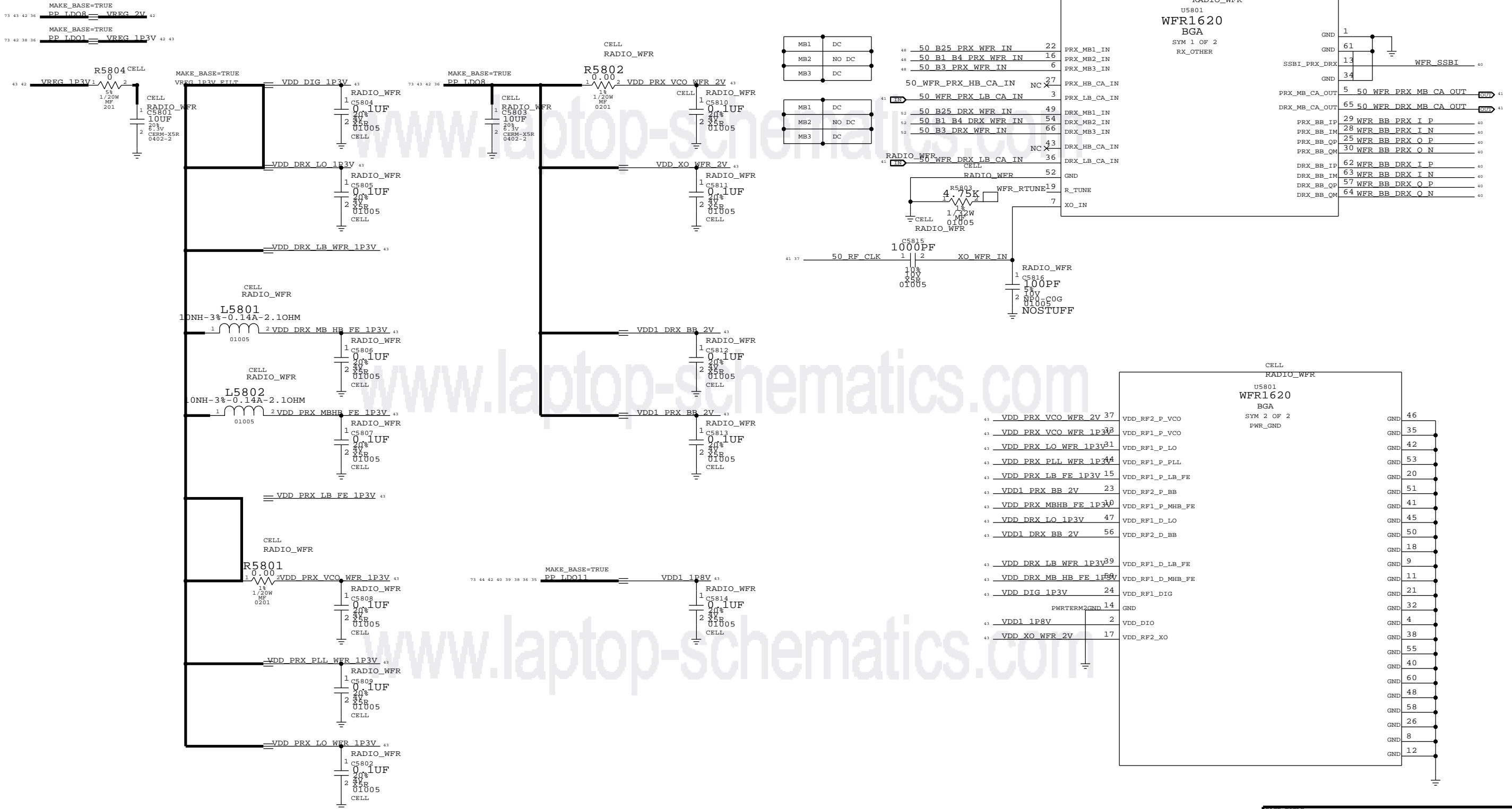



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C1019  
R1016  
L1000  
U1002



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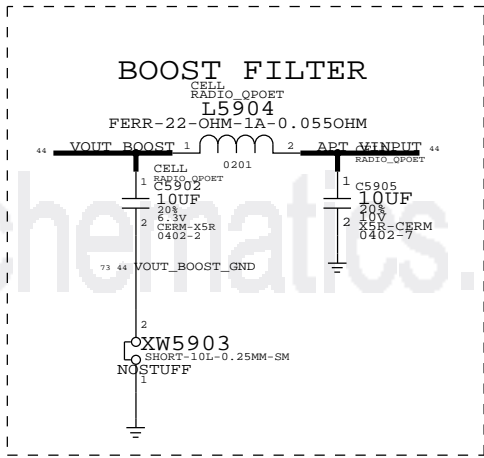
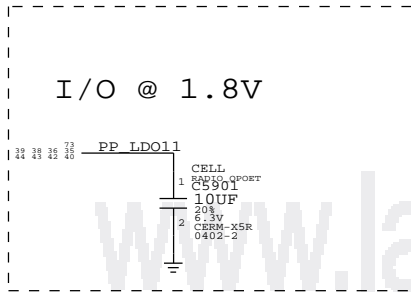
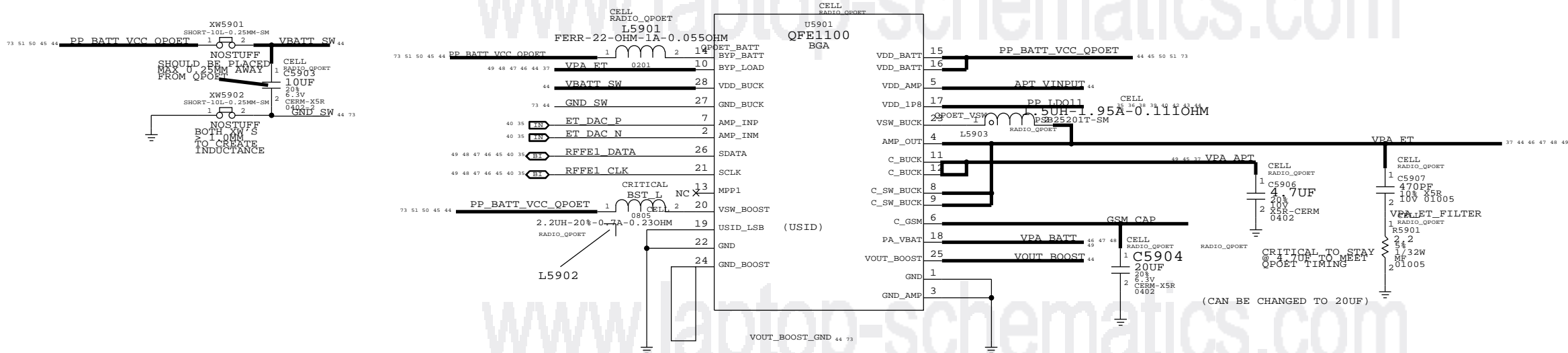
QFE

DCDC

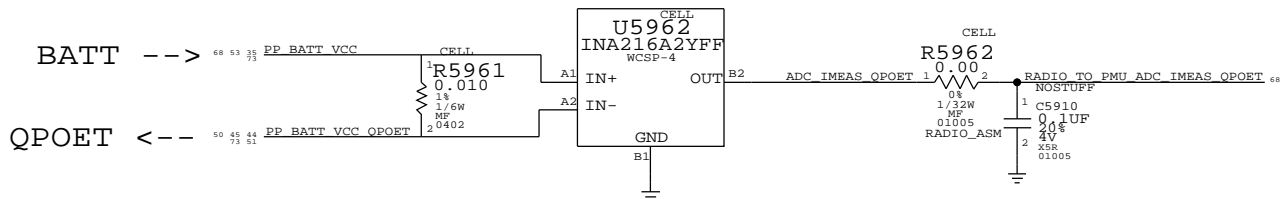
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C1110  
R1102  
L1104  
U1101

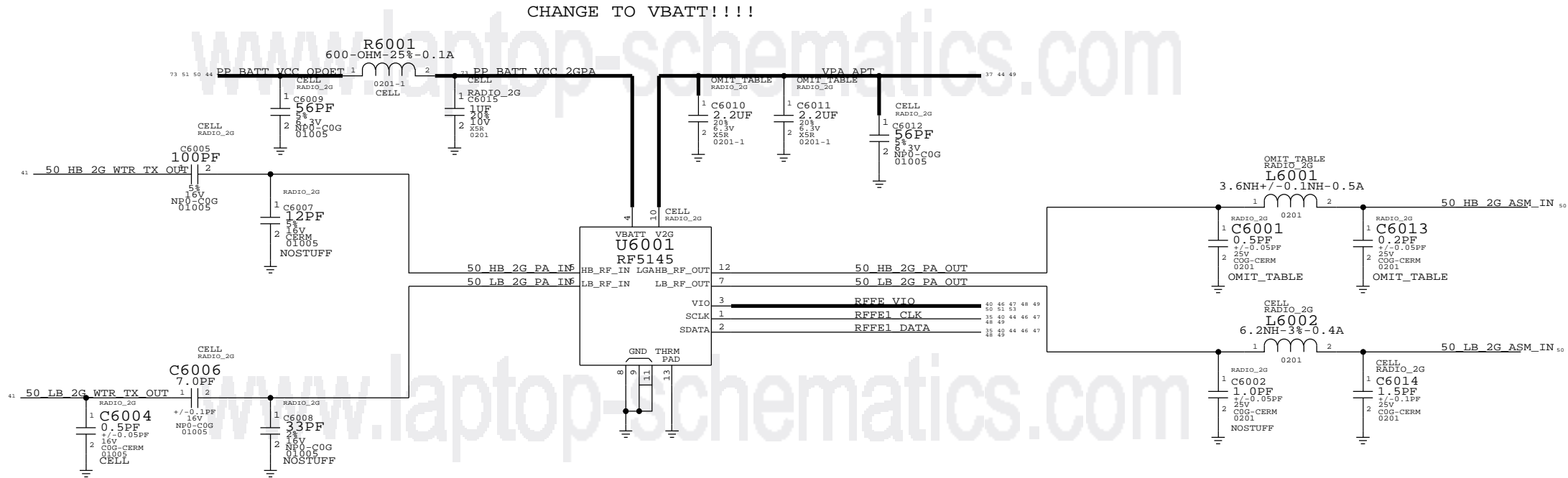


PP\_VCC\_MAIN CURRENT SENSE



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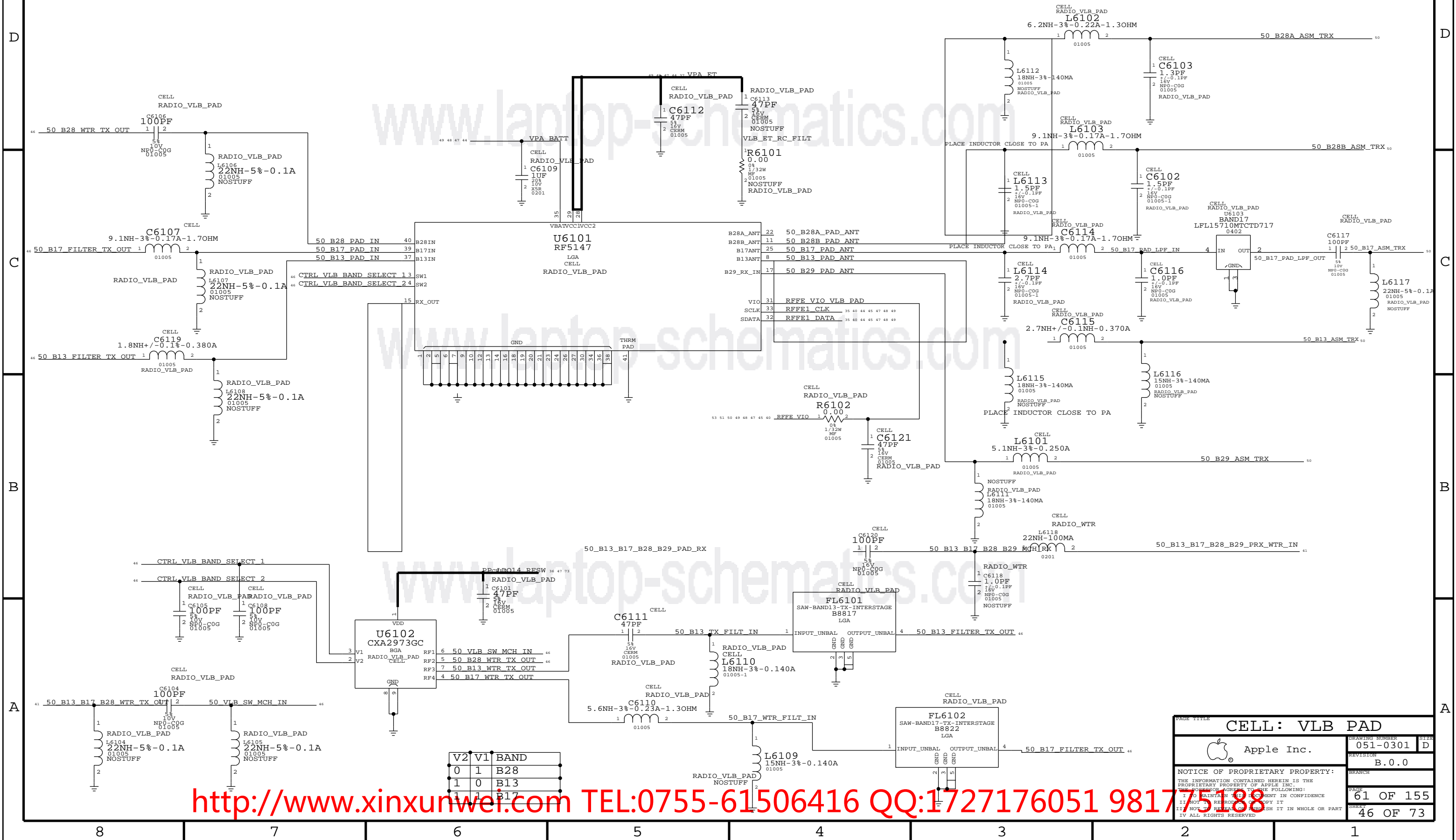
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# VERY LOW BAND PAD (B13, B17, B28)

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C1332  
R1300  
L4215\_RF  
U1304



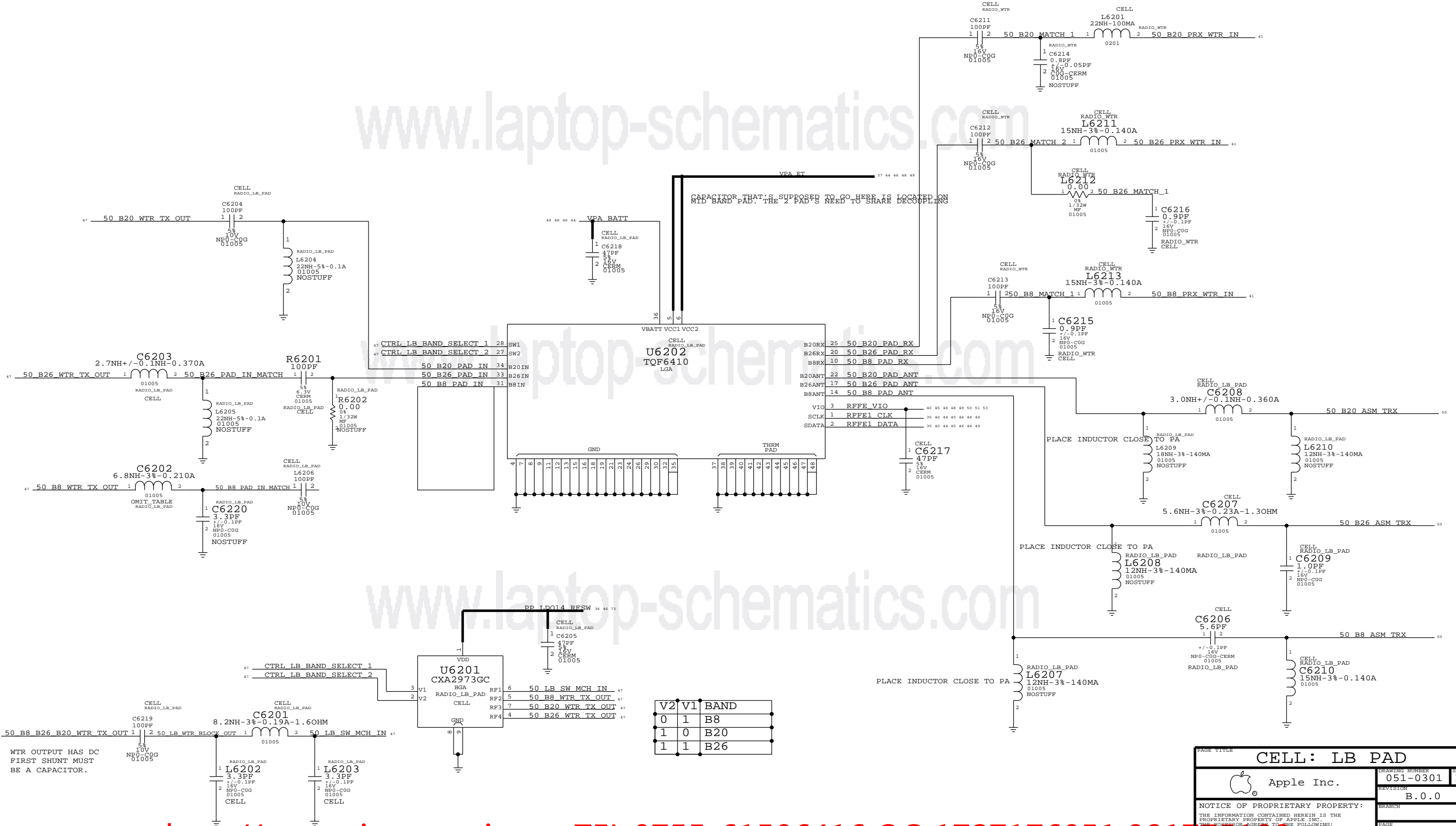
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LOW BAND PAD (B8, B26, B20)

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C4317_RF
R1400
L4316_RF
U1402



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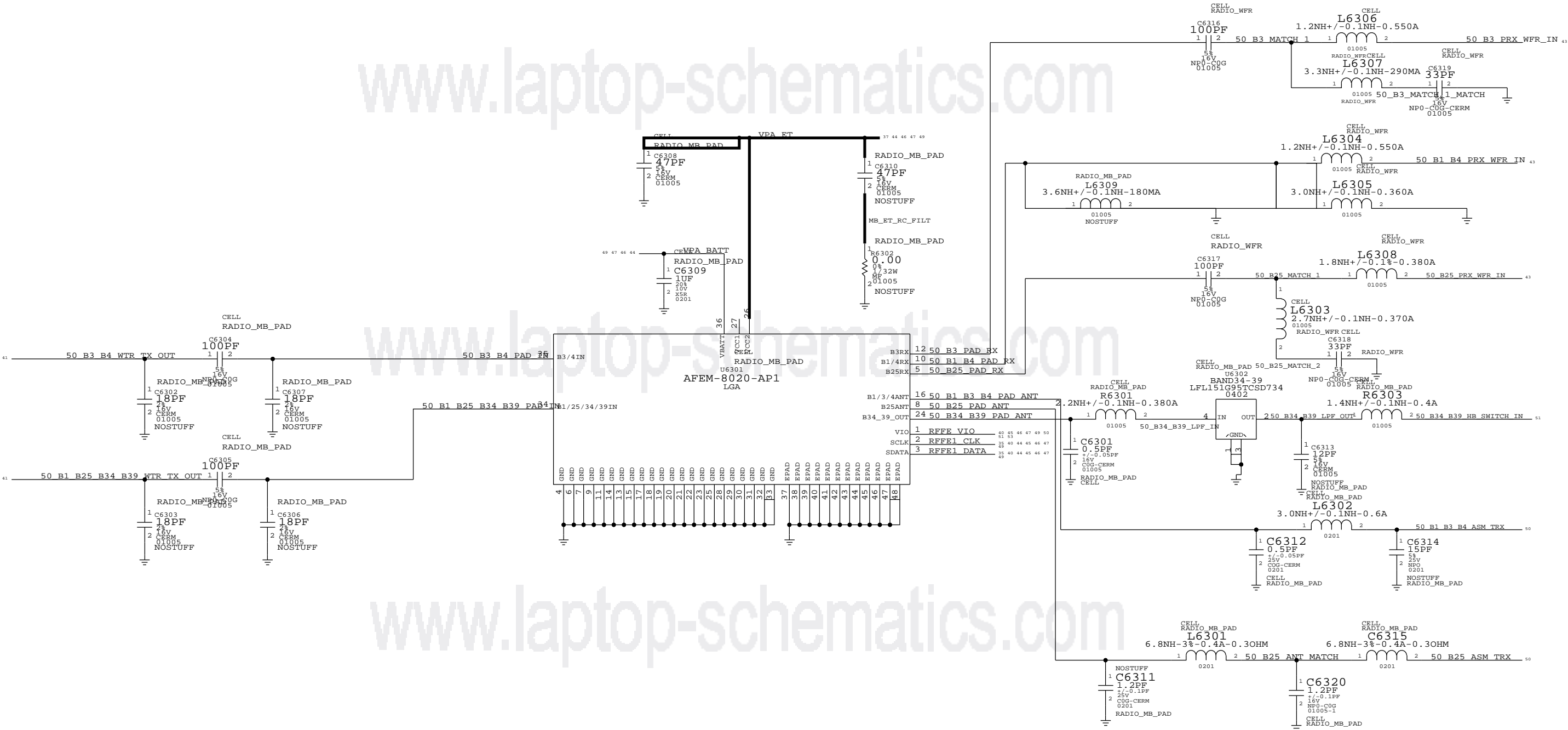
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	DRAWING NUMBER	051-0301
	REVISION	B.0.0
	BRANCH	
	PAGE	62 OF 155
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MID BAND PAD (B1, B25, B3, B4, B34, B39)

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C1510
R1500
L4409_RF
U1501

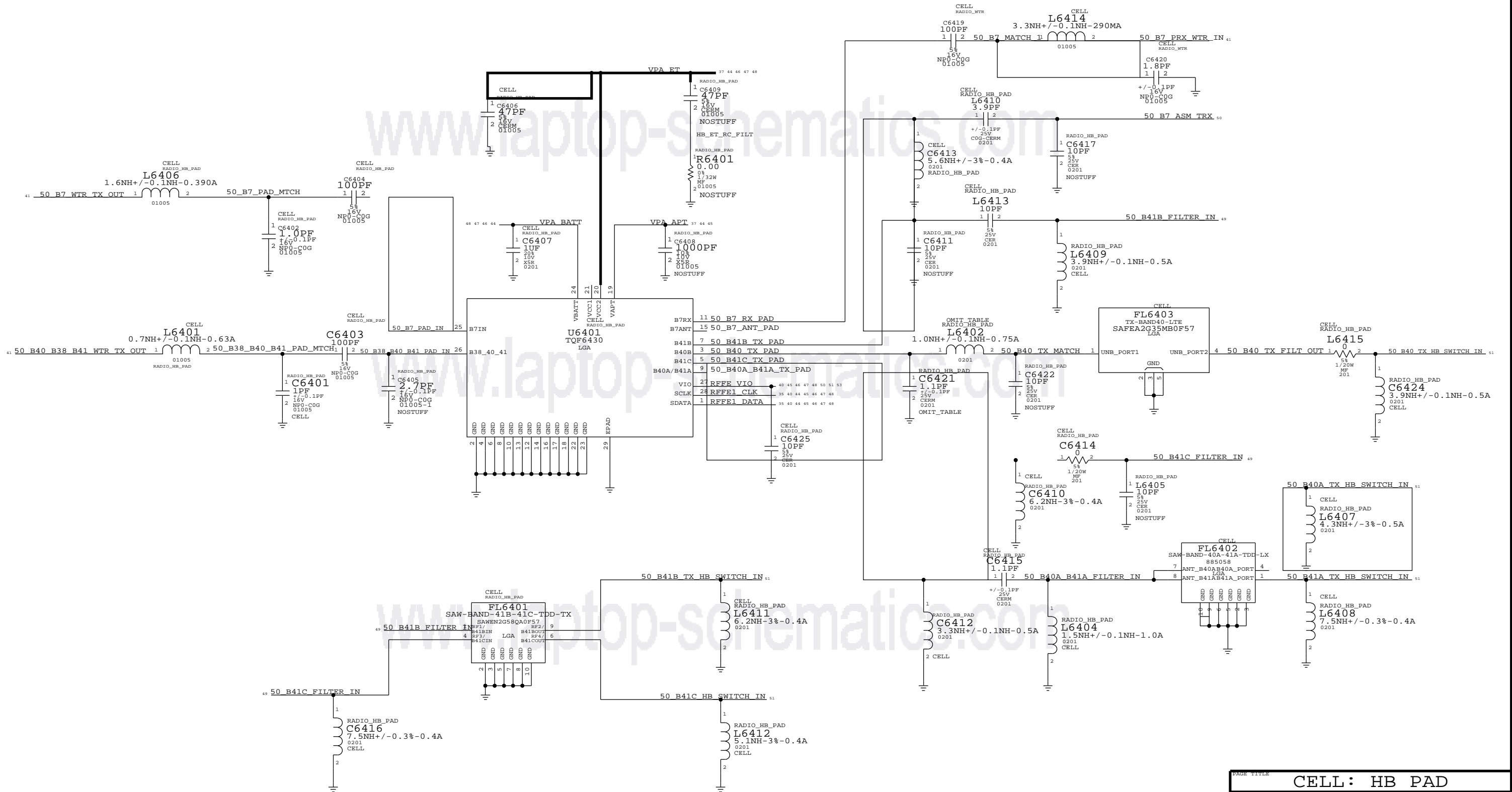



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	PAGE	63 OF 155
	SHEET	48 OF 73

HIGH BAND PAD (B38, B40, B41, XGP)

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C1614
R1600
L1616
U1601

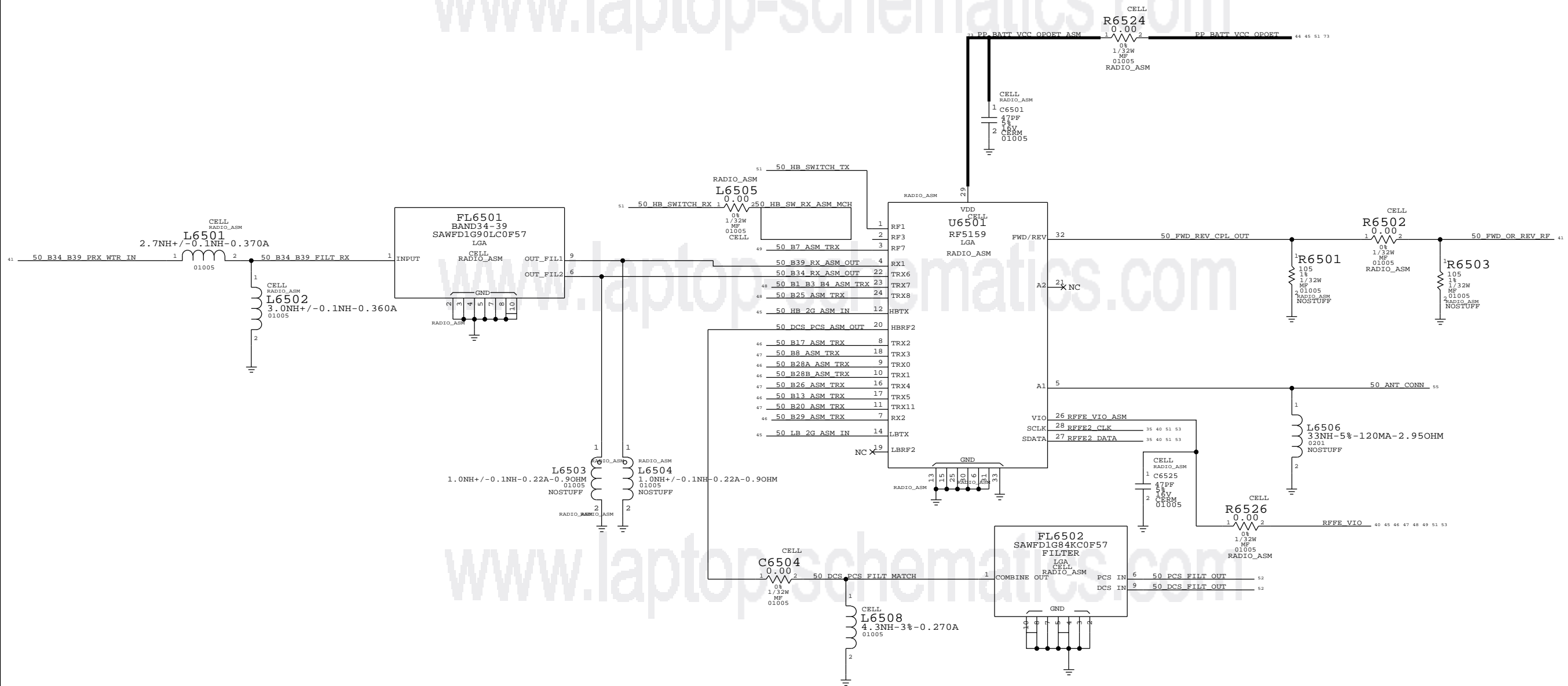



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		B.0.0	
1777-888		BRANCH	
		PAGE	
1777-888		64 OF 155	
		SHEET	
1777-888		49 OF 73	

ANTENNA SWITCH <http://www.xinxunwei.com> TEL:0755-61506416 QQ:1727176051 981775188

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C1702
R1700
L4608_RF
U1702



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		SHEET	50 OF 73

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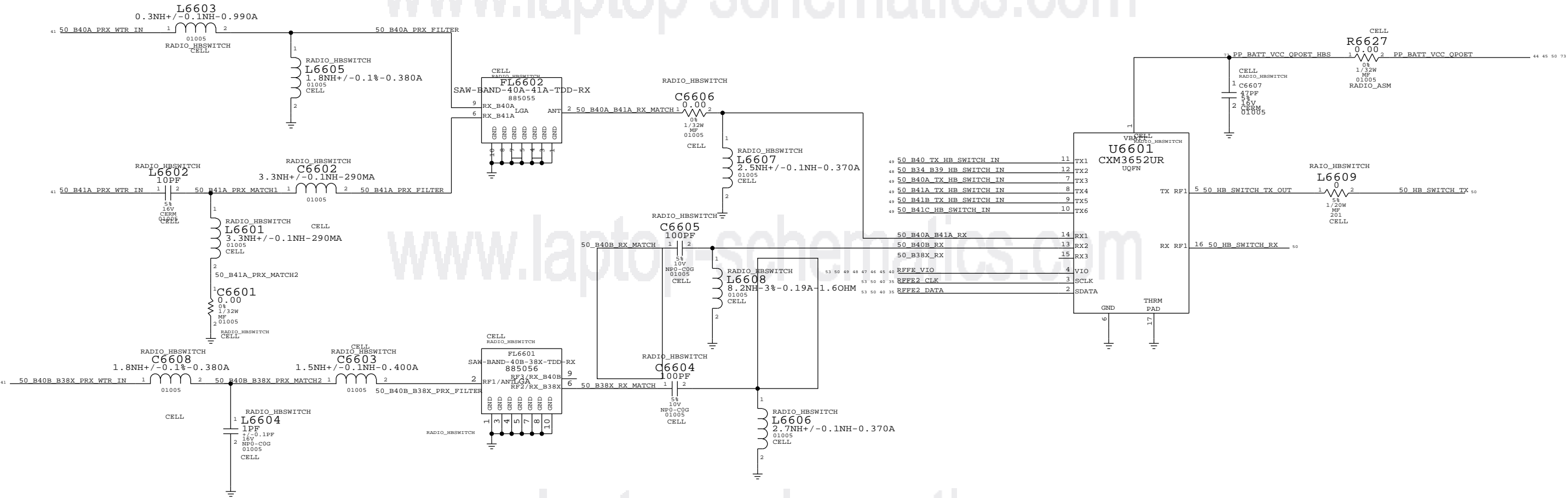
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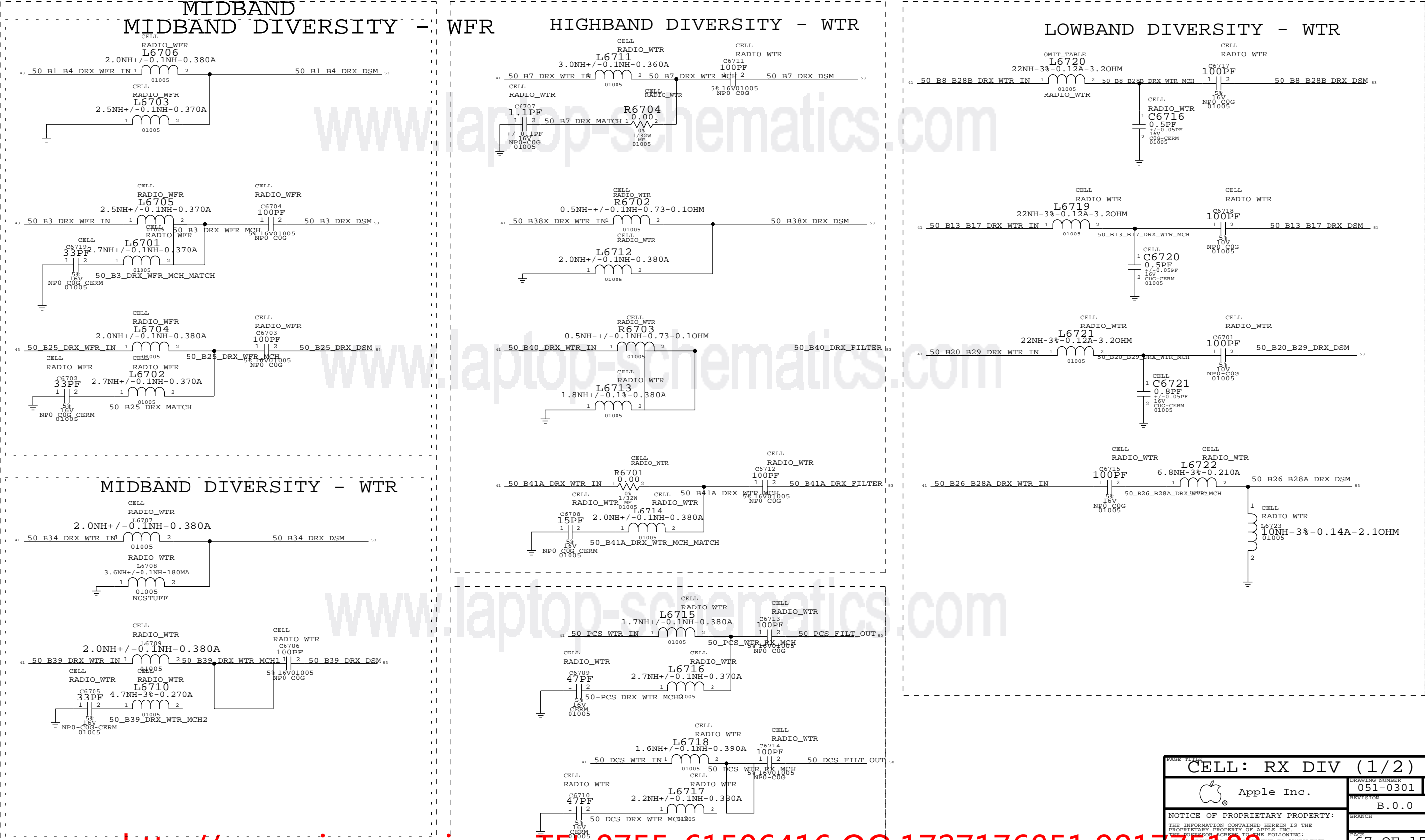


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	SHEET		51 OF 73

RX DIVERSITY (1 OF 2)

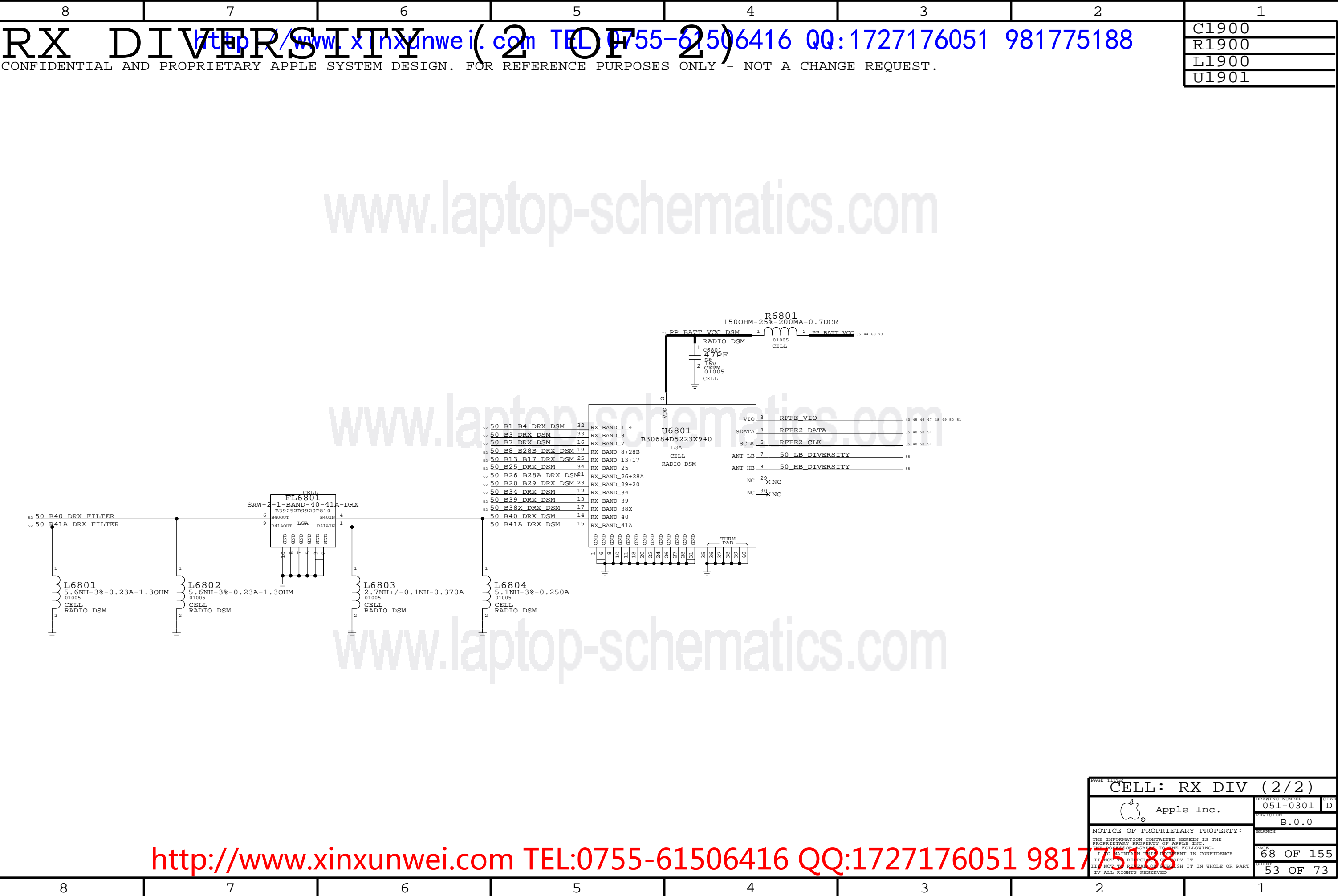
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C4826_RF
R1800
L1829
U1801



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GPS

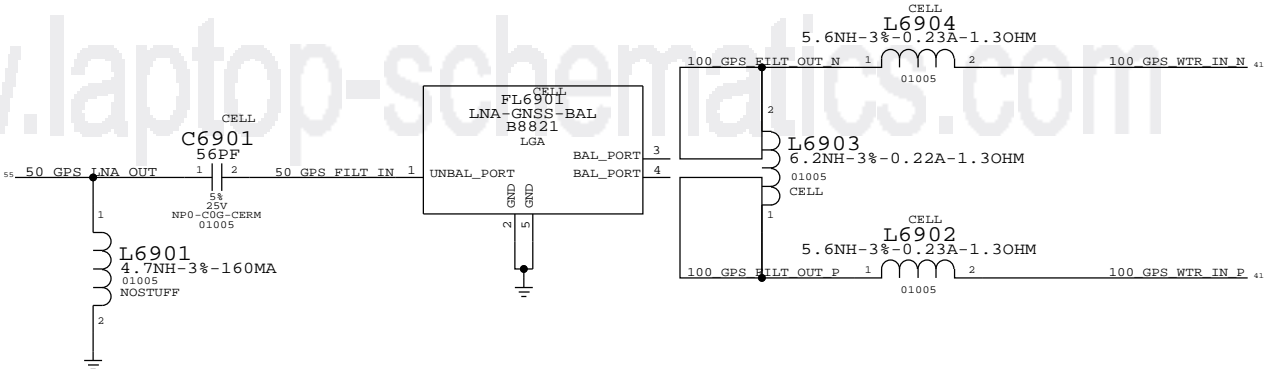
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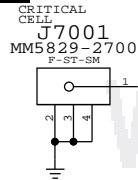
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		SHEET 54 OF 73

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# ANTENNA FEEDS AND GPS (J82)

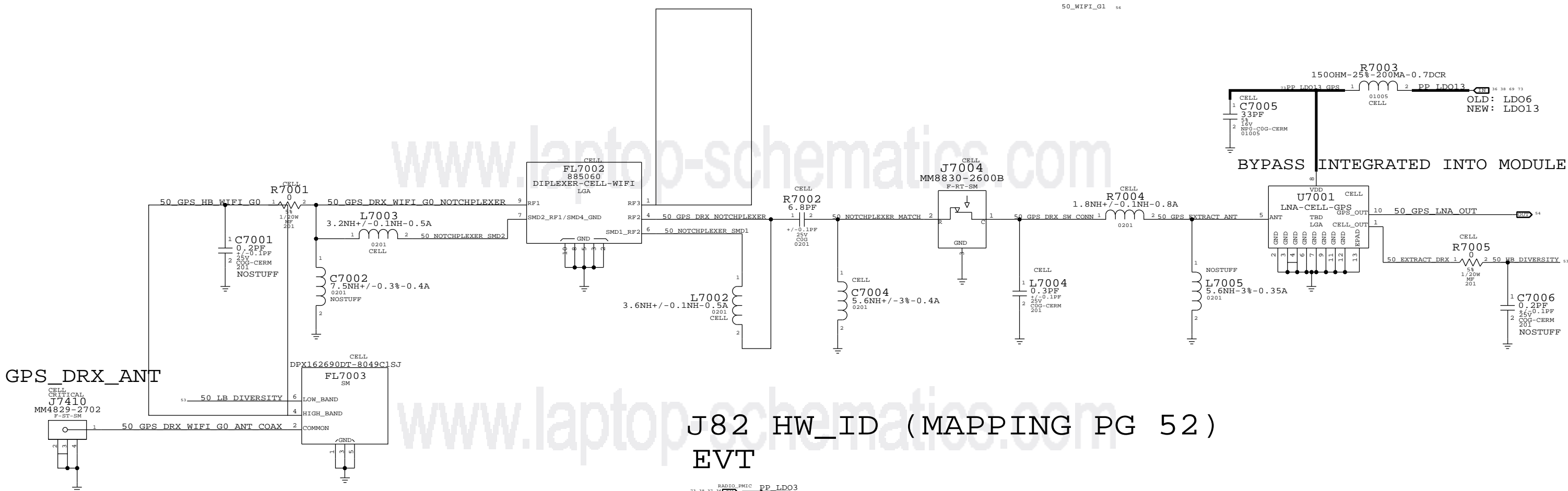
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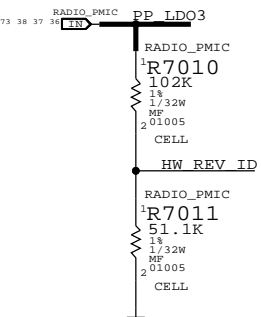
50\_WIFI\_G1



GPS\_DRX\_ANT

J82 HW\_ID (MAPPING PG 52)  
EVT

HW_REV_ID	R7010	R7011	J82 REV	J97 REV	J99 REV
0.10V	887K	51.1K	N/A	PROTO0	PROTO0
0.20V	422K	51.1K	PROTO0	PROTO0B	PROTO1
0.30V	255K	51.1K	PROTO1	PROTO1	PROTO2
0.40V	178K	51.1K	PROTO2		
0.50V	255K	100K	PRE-EVT		
0.60V	102K	51.1K	EVT		
0.70V	82.5K	51.1K	DVT		



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0565	197S0598		Y501	KDS XTAL, 19.2MHZ
197S0593	197S0598		Y501	NDK XTAL, 19.2MHZ

SYNC DATE=09/29/2014

CELL: ANT FEEDS & GPS (J82)

Apple Inc.

051-0301

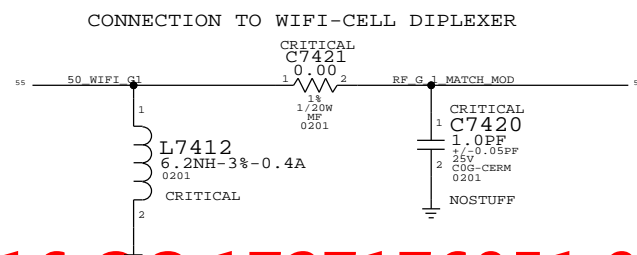
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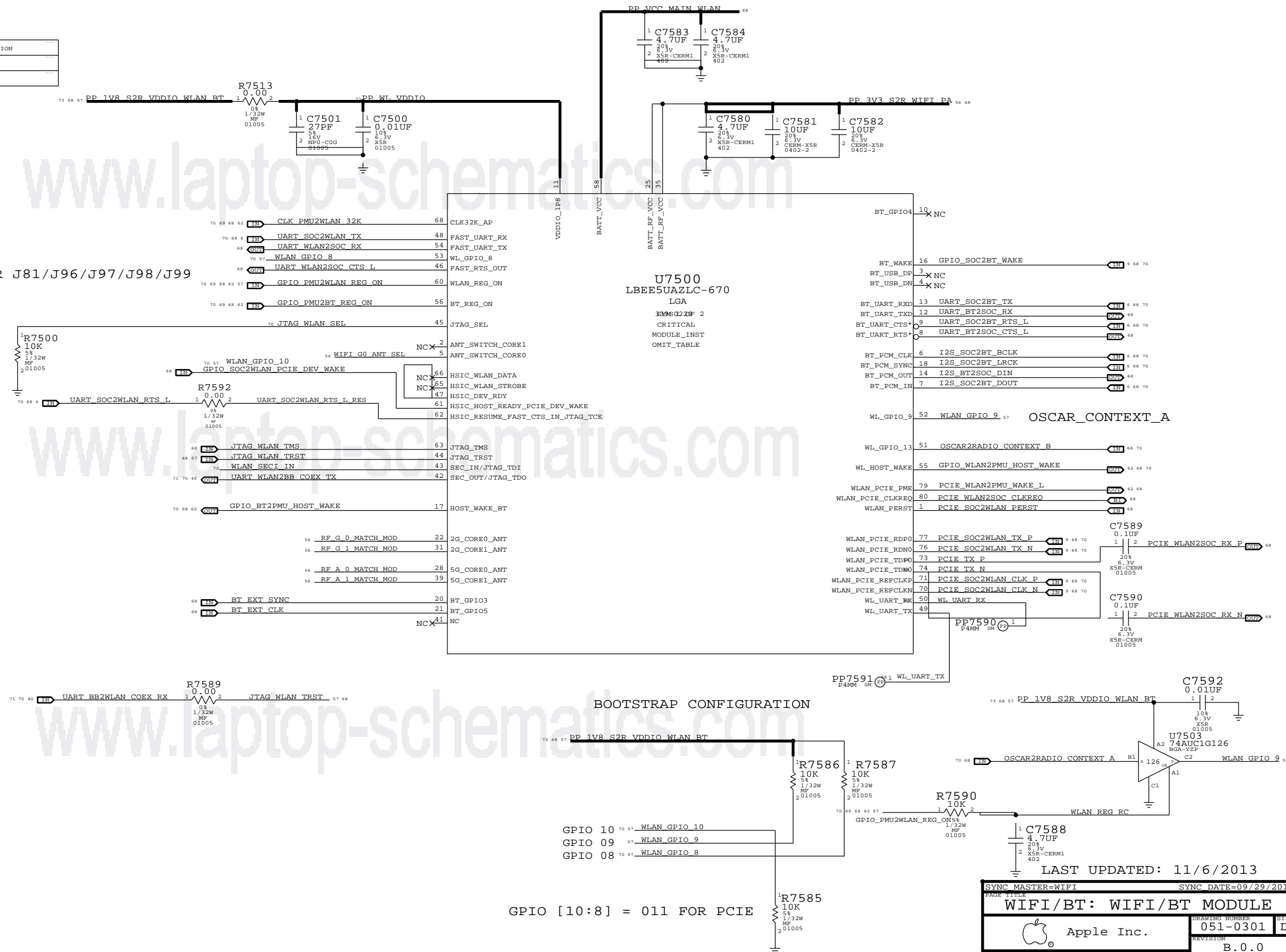


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WIFI/BT (3 OF 5) <http://www.xinkunwei.com> TEL:0755-61506416 QQ:1727176051 981775188

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
33980251	1	MODULE, WIFI/BT, STELLA CIDRE	U7500	CRITICAL	MLB_A
33980241	1	MODULE, WIFI/BT, STELLA	U7500	CRITICAL	MLB_B

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S0250	339S0251	MLB_A	U7500	STELLA CIDRE ALT
339S0229	339S0241	MLB_B	U7500	STELLA ALT



LAST UPDATED: 11/6/2013

SYNC MASTER=WIFI	SYNC DATE=09/29/2014
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WIFI/BT: WIFI/BT MODULE



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DRAWING NUMBER	SIZE
051-0301	D

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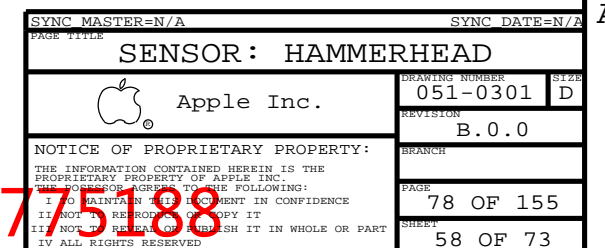
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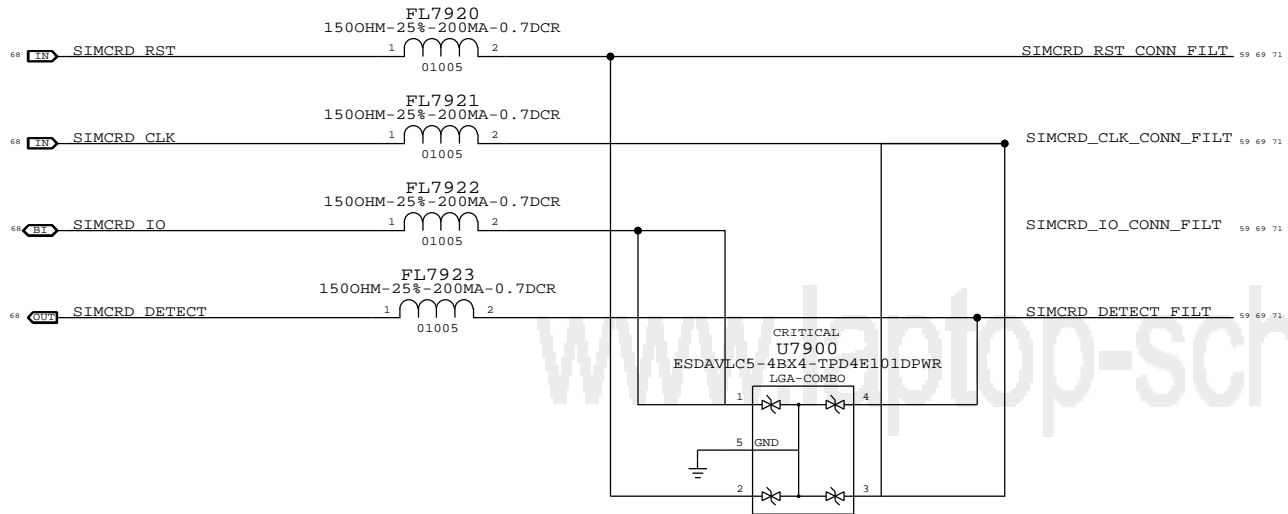
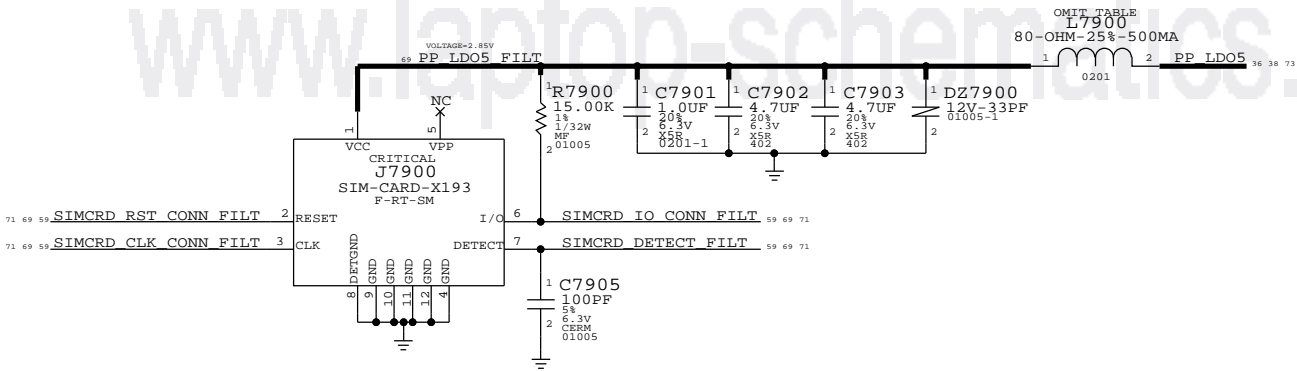
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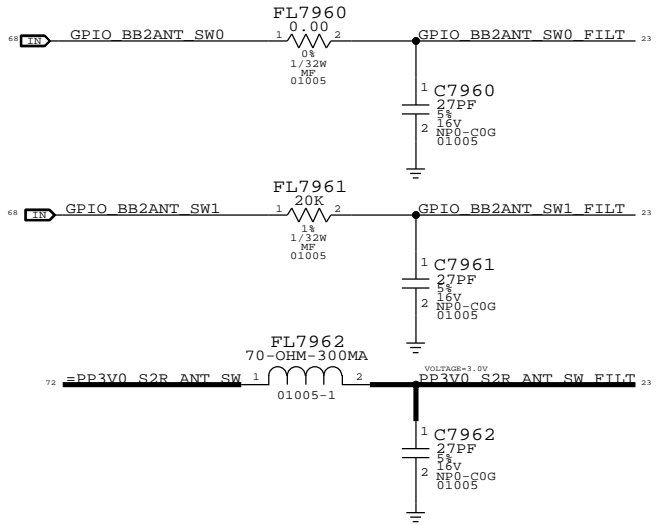



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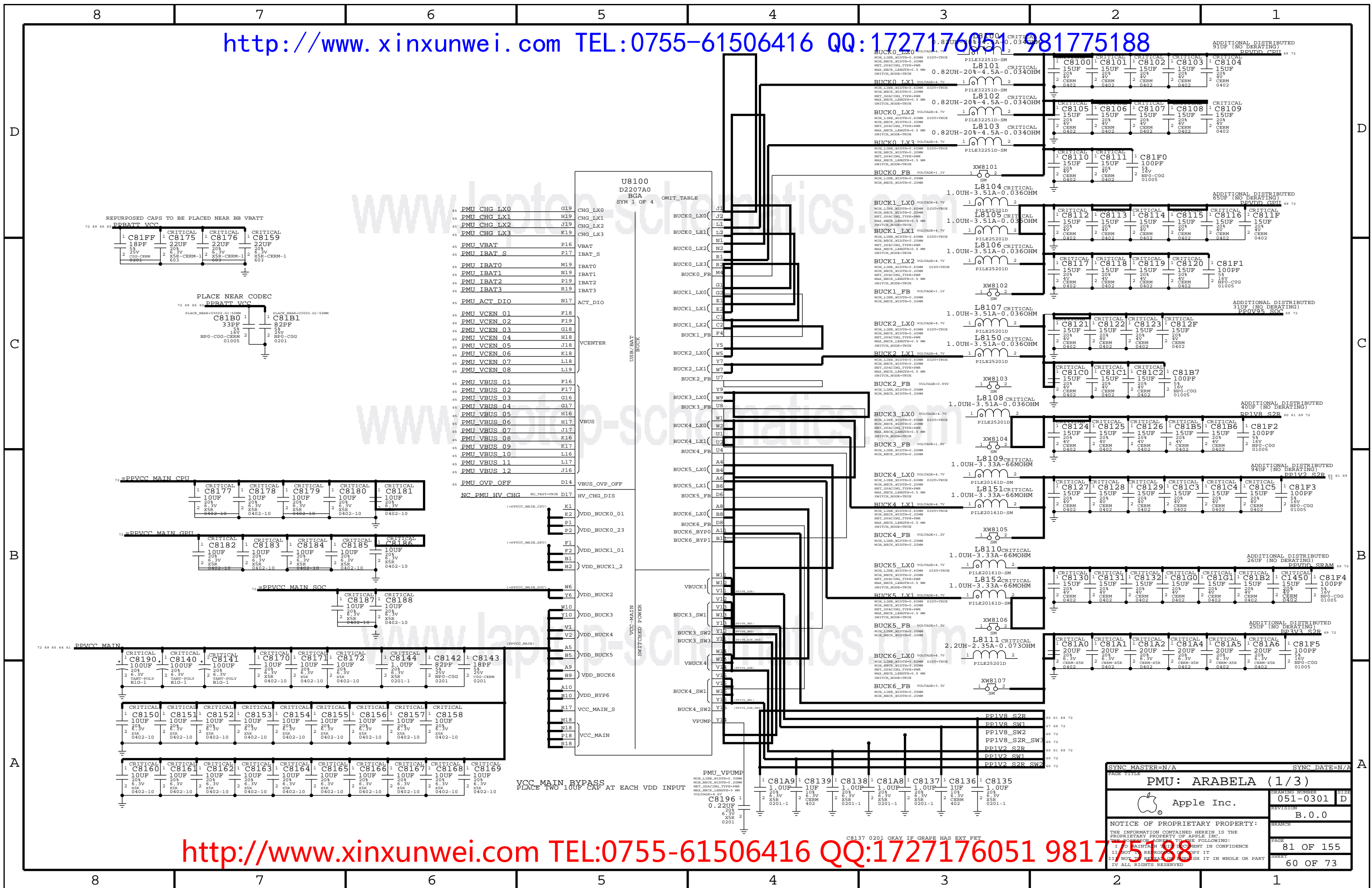
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
L55S00018		RESISTOR,800M,25%,500MA,0.1W	L7900	CRITICAL	



## ANTENNA SWITCH FILTERS



SYNC MASTER=N/A		SYNC DATE=N/A	
PAGE TITLE			
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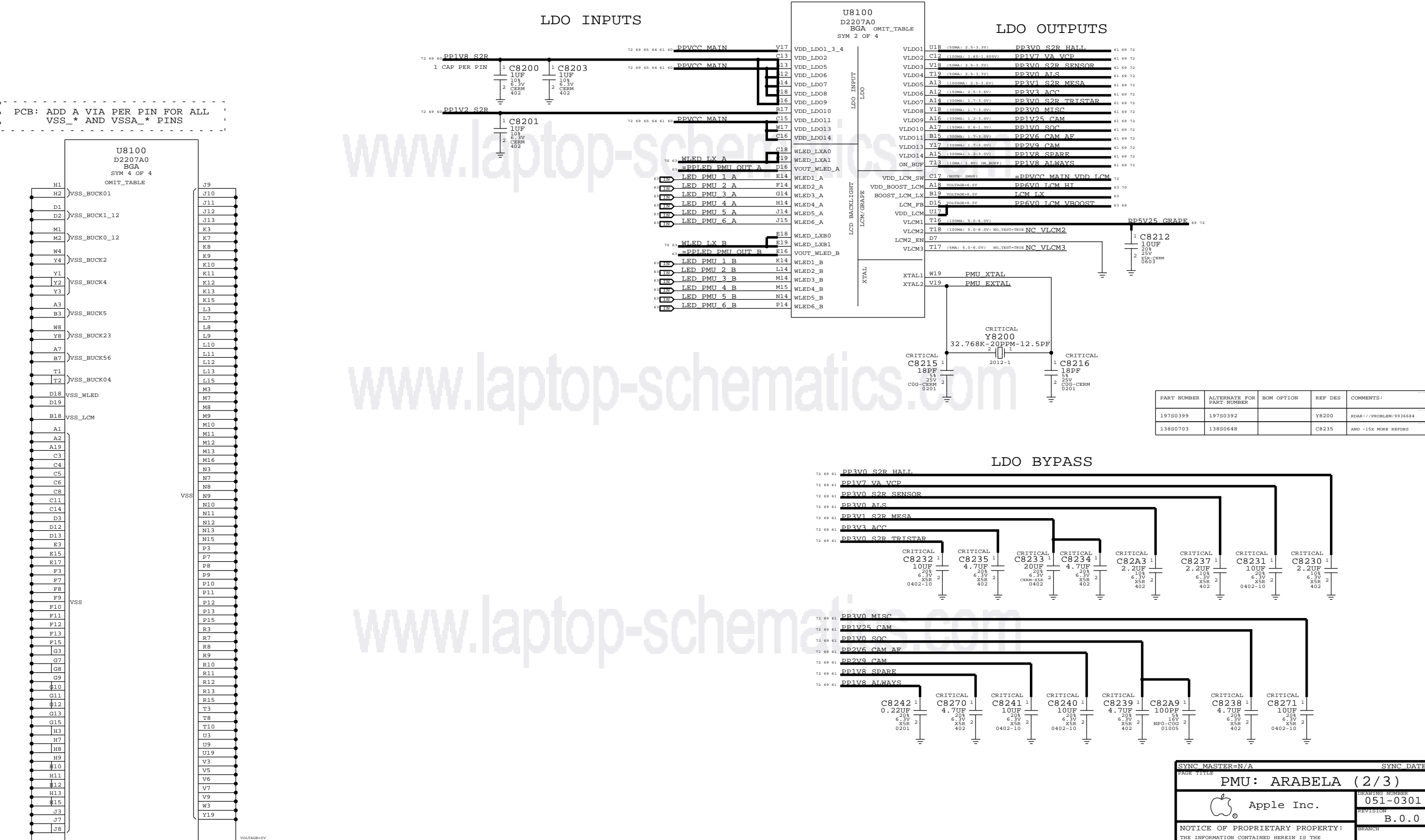
C

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PMU USB BRICKID R

ADC\_IN7

GPIO\_SOC2PMU KEEPACT

PMU SHDN

WD0G\_SOC2PMU RESET\_IN

BRICK\_ID

ADC\_IN7

ADC\_IN31

KEEPACT

SHDN

RESET\_IN1


DIGITAL

INVT

3.2k

CLK

WD0G

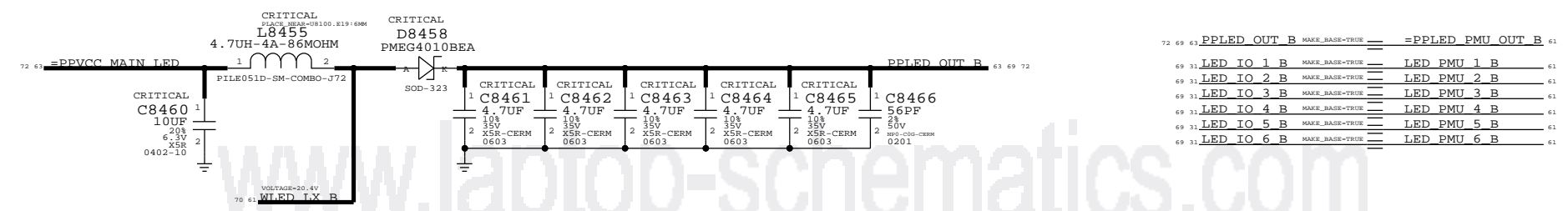
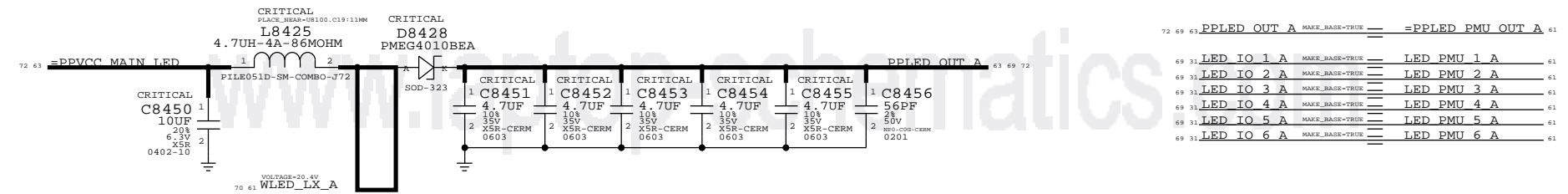
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PAGE TITLE PMU: ARABELA (3/3)			
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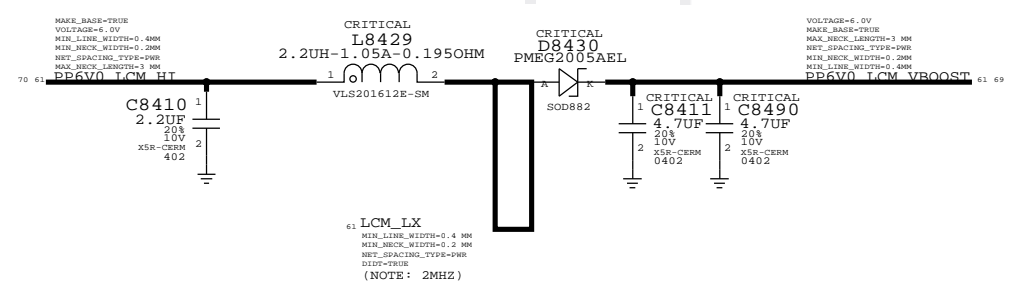



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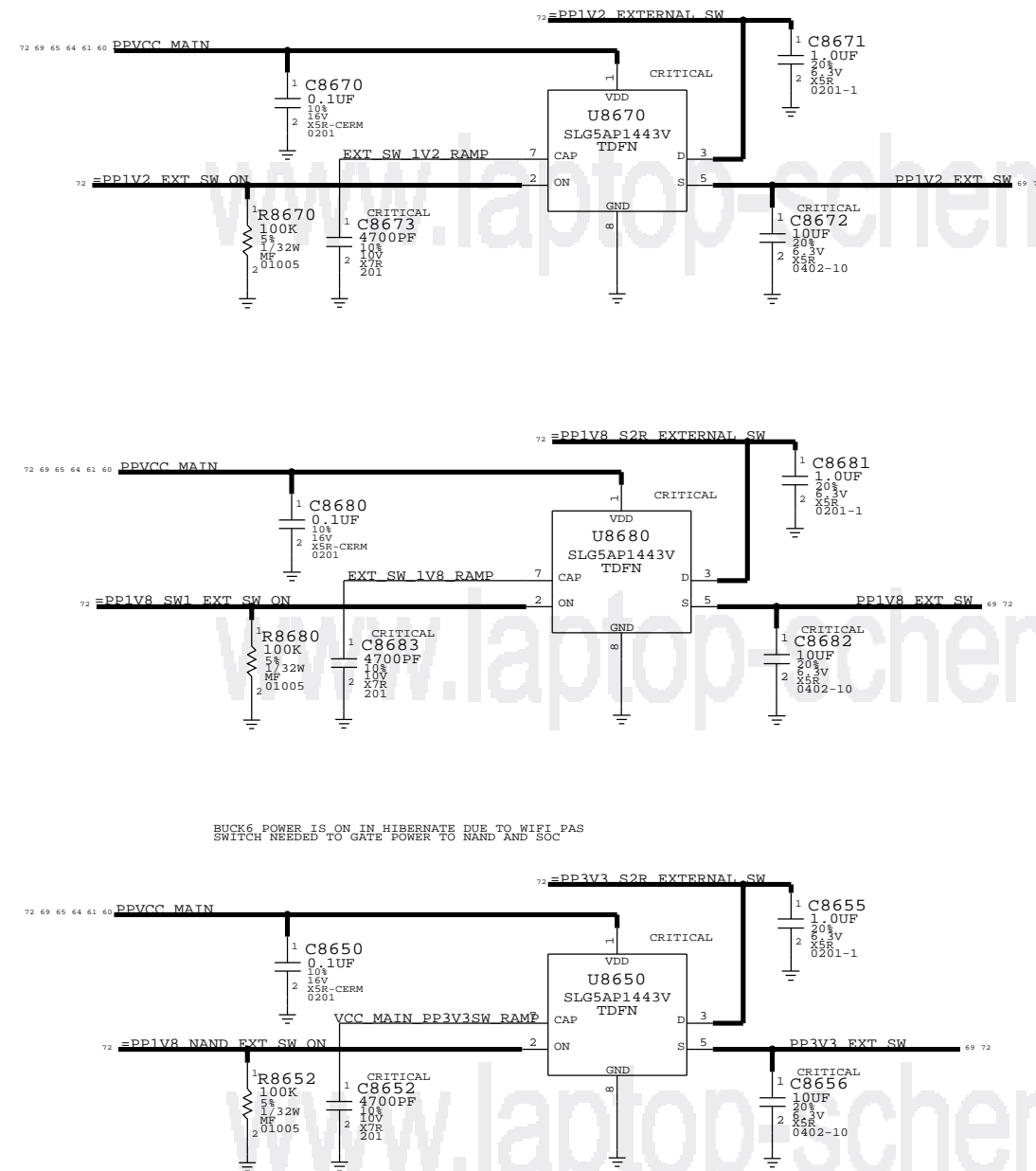
BACKLIGHT CIRCUIT MOVED HERE TO PERMIT SYNCING WITH DESIGNS USING BEACON




LCM BOOST MOVED HERE TO PERMIT SYNCING WITH DESIGNS USING KONA



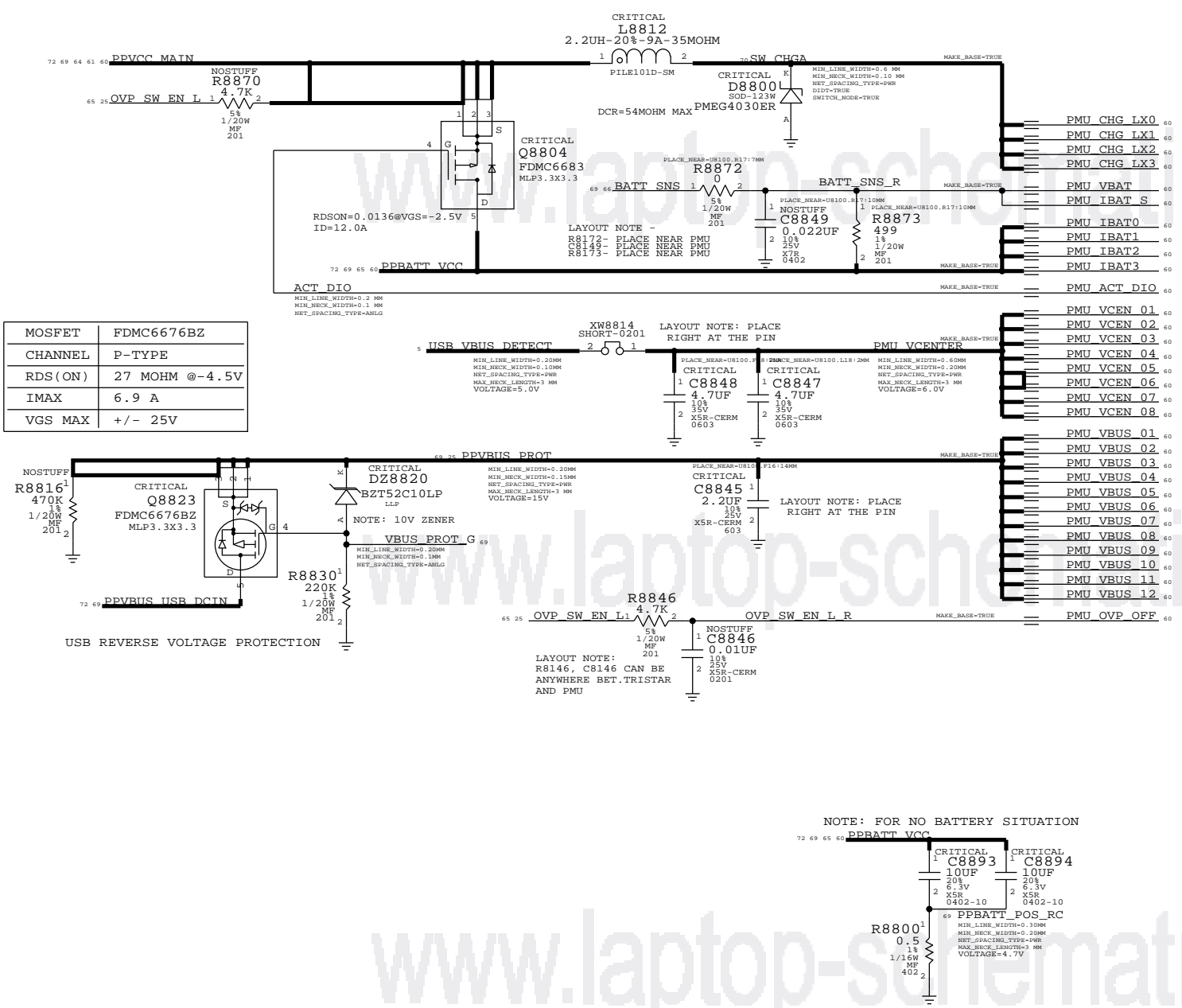
SYNC MASTER=N/A		SYNC DATE=N/A	
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POWER: J82 SPECIFIC			
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		PAGE	84 OF 155
		SHEET	63 OF 73



BUCK6 POWER IS ON IN HIBERNATE DUE TO WIFI PAS  
SWITCH NEEDED TO GATE POWER TO NAND AND SOC

SYNC MASTER=N/A		SYNC DATE=N/A	
PAGE TITLE			
POWER: EXTERNAL SWITCHES			
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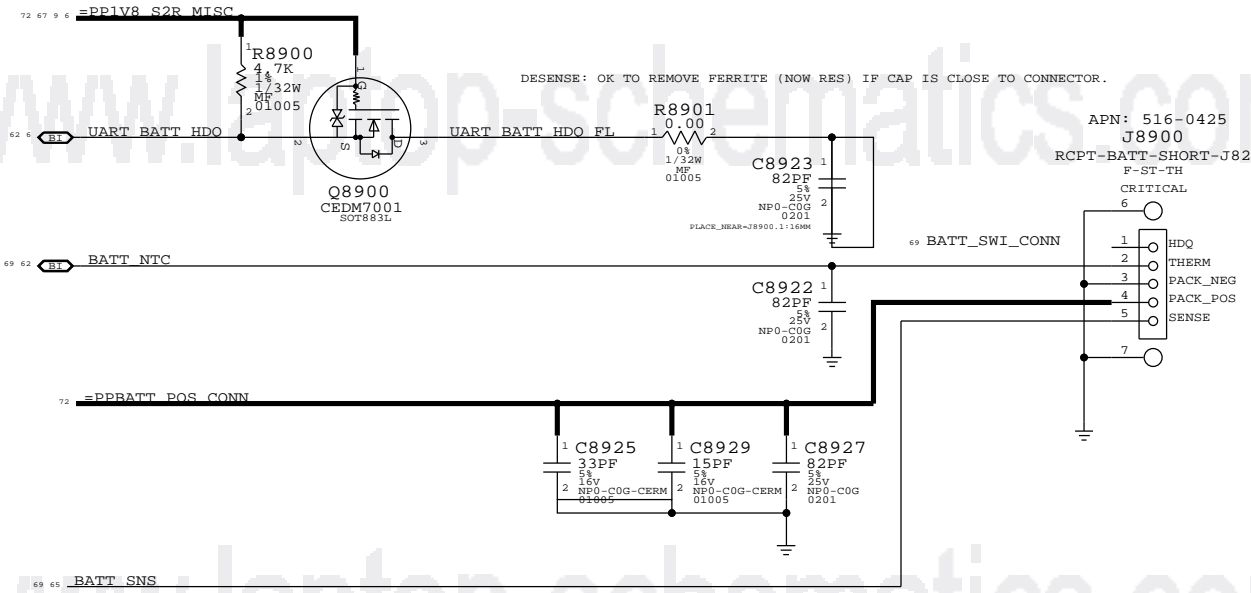
REV	DATE	DESCRIPTION	BY	CHK
1	2015-03-01	PMU: CHARGER BUCK	051-0301	D



MOSFET	FDMC6676BZ
CHANNEL	P-TYPE
RDS(ON)	27 MOHM @ -4.5V
IMAX	6.9 A
VGS MAX	+/- 25V

PMU: CHARGER BUCK		051-0301	D
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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
15580644	15580823		FL8900	EDASH // PROBLEM 11282301

SYNC MASTER=N/A

SYNC DATE=N/A

POWER: BATTERY CONN

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66 OF 73

DEBUG RESET ACCESS





# BASEBAND

## GPIO

71	69	6	GPIO SOC2BB RADIO ON L	MAKE_BASH+TRIM	RADIO ON L	GPIO	35	37	
		6	GPIO SOC2BB RESET L	MAKE_BASH+TRIM	BB RST L	GPIO	35	37	
	69	6	GPIO BB2SOC RESET DET L	MAKE_BASH+TRIM	BB RESET DET L	GPIO	35	40	
71	70	69	62	GPIO PMU2BBPMU RESET L	MAKE_BASH+TRIM	RF PMIC RESET L	GPIO	35	37
71	6	GPIO SOC2BB WAKE MODEM	MAKE_BASH+TRIM	AP WAKE MODEM	GPIO	35	37		
70	69	62	25	10	5	4	RESET SOC L	GPIO	35
71	6	GPIO SOC2BB COREDUMP	MAKE_BASH+TRIM	BB CORE DUMP	GPIO	35	37		
	6	GPIO BB IPC	MAKE_BASH+TRIM	BB IPC GPIO	GPIO	35	40		
71	6	GPIO BB2SOC GPS SYNC	MAKE_BASH+TRIM	BB GPS SYNC	GPIO	35	40		
70	69	62	GPIO BB2PMU HOST WAKE L	MAKE_BASH+TRIM	BB WAKE HOST	GPIO	35	40	

## UART

71	26	UART_BB2SOC_TX	MAKE_BASE=TRUE	BB_UART_TXD	35	40
71	26	UART_SOC2BB_TX	MAKE_BASE=TRUE	BB_UART_RXD	35	40
71	26	UART_BB2SOC_RTS_L	MAKE_BASE=TRUE	BB_UART_RTS_L	35	40
71	26	UART_SOC2BB_RTS_L	MAKE_BASE=TRUE	BB_UART_CTS_L	35	40
71	17	UART_OSCAR2BB_TX	MAKE_BASE=TRUE	BB_OTHER_RXD	40	40
71	17	UART_BB2OSCAR_TX	MAKE_BASE=TRUE	BB_OTHER_TXD	40	40

## HSIC

69	6	HSIC_SOC2BB_HOST_RDY	MAKE_BAISE=TRUE	BB_HOST_RDY	35 40
69	6	HSIC_BB2SOC_DEVICE_RDY	MAKE_BAISE=TRUE	BB_DEVICE_RDY	35 40
71	5	HSIC_BB_DATA	MAKE_BAISE=TRUE	50 BB_HSIC_DATA	35 39
71	5	HSIC_BB_STB	MAKE_BAISE=TRUE	50 BB_HSIC_STROBE	35 39

## USB

Line	Signal	Direction	Value
71 69 62	GPIO PMU2BB VRUS DET	IN	0
71 25	USB BB P	BI	0
71 25	USB BB N	BI	0

## SIM CARD

Signal	Direction	Source	Destination	Width
59	SEN	SIMCRD_DETECT	BB_SIM_DETECT	39
59	OUTEN	SIMCRD_RST	BB_SIM_RESET	40
59	OUTEN	SIMCRD_CLK	BB_SIM_CLK	40
55	SEN	SIMCRD_IO	BB_SIM_DATA	40

## ADC

62	<b>OUT3</b>	ADC BB2PMU IMEAS RADIO	NAKE_BASE=TRUE	=====	RADIO TO PMU ADC IMEAS RADIO	<b>IN</b>	35
62	<b>OUT1</b>	ADC BB2PMU IMEAS OPOET	NAKE_BASE=TRUE	=====	RADIO TO PMU ADC IMEAS OPOET	<b>IN</b>	44

## POWER

```
72  =PPBATT VCC BB                                     PP BATT VCC 35 44 53 73
```

LOWER ANT CTRL

59 **OUT** GPIO\_BB2ANT\_SW0 MAKE\_BASE=TRUE == BB\_ANTSW\_GPIO0 **IN** 40

59 **OUT** GPIO\_BB2ANT\_SW1 MAKE\_BASE=TRUE == BB\_ANTSW\_GPIO1 **IN** 40

WLAN / BT  
GPIO

Time	Device	Message	Value	Time	Device	Message	Value
70.69.68.62.57	BCM	CLK PMU2WLAN 32K	MAKE_BASE+TRUE		BCM	CLK PMU2WLAN 32K	57.62.68.69.70
70.69.68.62.57	BCM	GPIO PMU2BT REG ON	MAKE_BASE+TRUE		BCM	GPIO PMU2BT REG ON	57.62.68.69.70
70.69.68.62.57	BCM	GPIO PMU2WLAN REG ON	MAKE_BASE+TRUE		BCM	GPIO PMU2WLAN REG ON	57.62.68.69.70
70.68.57.9	BCM	GPIO SOC2BT WAKE	MAKE_BASE+TRUE		BCM	GPIO SOC2BT WAKE	9.57.68.70
70.9	BCM	GPIO SOC2WLAN WAKE	MAKE_BASE+TRUE		BCM	GPIO SOC2WLAN PCIE DEV WAKE	57
70.68.62.57	BCM	GPIO BT2PMU HOST WAKE	MAKE_BASE+TRUE		BCM	GPIO BT2PMU HOST WAKE	57.62.68.70
70.68.62.57	BCM	GPIO WLAN2PMU HOST WAKE	MAKE_BASE+TRUE		BCM	GPIO WLAN2PMU HOST WAKE	57.62.68.70

## PCI-E

[illegible]

## UART

70	68	57	6	UART SOC2BT TX	MAKE_BASE+731E	UART SOC2BT TX	6	57	68	70
70	68	57	6	UART SOC2BT RTS L	MAKE_BASE+731E	UART SOC2BT RTS L	6	57	68	70
70	6	UART BT2SOC TX	MAKE_BASE+731E	UART BT2SOC RX				57		
70	6	UART BT2SOC RTS L	MAKE_BASE+731E	UART BT2SOC CTS L				57		

Line	File	Code	Symbol	Value	Symbol	Value
70	68	57	UART_S0C2WLAN_TX	MAKE_BASE_TRUE	UART_S0C2WLAN_TX	68 57 70
70	68	57	UART_S0C2WLAN_RTS_L	MAKE_BASE_TRUE	UART_S0C2WLAN_RTS_L	68 57 70
70	68	57	UART_WLAN2SOC_TX	MAKE_BASE_TRUE	UART_WLAN2SOC_TX	57
70	68	57	UART_WLAN2SOC_RTS_L	MAKE_BASE_TRUE	UART_WLAN2SOC_RTS_L	57

OR IN NAME	TP	WL	UART	RX	MAKE_BASE=TRUE	WL	UART	RX	57
	TP	WL	UART	TX	MAKE_BASE=TRUE	WL	UART	TX	57

I2S

70	CPU0	I2S_BT2SOC_DOUT	MAKES_BASE-TWICE	I2S_BT2SOC_DIN	CPU0	57
70	68 57	I2S_SOC2BT_DOUT	MAKES_BASE-TWICE	I2S_SOC2BT_DOUT	CPU0	6 57 68 70
70	68 57	I2S_SOC2BT_RCLK	MAKES_BASE-TWICE	I2S_SOC2BT_RCLK	CPU0	6 57 68 70
70	68 57	I2S_SOC2BT_LRCK	MAKES_BASE-TWICE	I2S_SOC2BT_LRCK	CPU0	6 57 68 70

## OSCAR CONTEXT



```

17  [IN]  GPIO OSCAR2WLAN CONTEXT A  MAKE_BASE=TRUE  ==  OSCAR2RADIO CONTEXT A  [OUT]  57 70
17  [IN]  GPIO OSCAR2WLAN CONTEXT B  MAKE_BASE=TRUE  ==  OSCAR2RADIO CONTEXT B  [OUT]  57 70

```

## JTAG

70  TP JTAG WLAN TMS MAKE\_BASE=TRUE  JTAG WLAN TMS 57

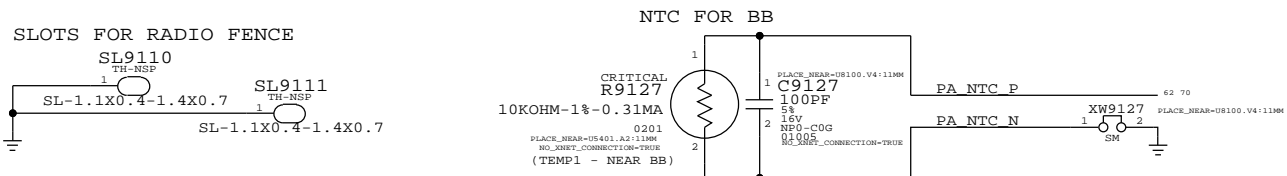
70  TP JTAG WLAN TRST MAKE\_BASE=TRUE  JTAG WLAN TRST 57


## POWER

72	=PPVCC MAIN WLAN	PP VCC MAIN WLAN	57
72	=PP3V3 S2R WIFI PA	PP 3V3 S2R WIFI PA	56 57
72	=PP1V8 S2R VDDIO WLAN BT	PP 1V8 S2R VDDIO WLAN BT	57 73

NO CONNECT

NC WLAN GPIO3	NO_TEST=TRUE	MAKE_BASE=TRUE	BT_EXT_SYNC	57
NC WLAN GPIO5	NO_TEST=TRUE	MAKE_BASE=TRUE	BT_EXT_CLK	57



SYNC MASTER=N/A		SYNC DATE=N/A	
PAGE TITLE			
ALIASES: BB/WLAN/BT			
 Apple Inc.	DRAWING NUMBER	SIZE	
	051-0301	D	
	REVISION		
	B.0.0		
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		SHEET 68 OF 73	

POWER - BUCKS

PPVDD CPU	FUNC_TEST=TRUE	60 72
PPVDD GPU	FUNC_TEST=TRUE	60 72
PPV95 SOC	FUNC_TEST=TRUE	60 72
PPV8 S2R	FUNC_TEST=TRUE	60 61 72
PPV8 SW1	FUNC_TEST=TRUE	60 67 72
PPV8 SW1 FOREHEAD	FUNC_TEST=TRUE	72
PPV8 EXT SW	FUNC_TEST=TRUE	64 72
PPV8 SW2	FUNC_TEST=TRUE	60 72
PPV8 GRAPE EXT SW	FUNC_TEST=TRUE	30 72
PPV8 S2R SW3	FUNC_TEST=TRUE	60 72
PPV2 S2R	FUNC_TEST=TRUE	60 61 72
PPV2 SW1	FUNC_TEST=TRUE	60 72
PPV2 EXT SW	FUNC_TEST=TRUE	64 72
PPV2 S2R SW2	FUNC_TEST=TRUE	60 72
PPVDD SRAM	FUNC_TEST=TRUE	60 72
PPV3 S2R	FUNC_TEST=TRUE	60 72
PPV3 EXT SW	FUNC_TEST=TRUE	64 72

POWER - LDOS

PPV7 VA VCP	FUNC_TEST=TRUE	61 72
PPV0 S2R SENSOR	FUNC_TEST=TRUE	61 72
PPV0 ALS	FUNC_TEST=TRUE	61 72
PPV3 ACC	FUNC_TEST=TRUE	61 72
PPV0 S2R TRISTAR	FUNC_TEST=TRUE	61 72
PPV1 S2R MESA	FUNC_TEST=TRUE	61 72
PPV0	FUNC_TEST=TRUE	61 72
PPV8 SPARE	FUNC_TEST=TRUE	61 72
PPV0 S2R HALL	FUNC_TEST=TRUE	61 72
PPV0 MISC	FUNC_TEST=TRUE	61 72
PPV25 CAM	FUNC_TEST=TRUE	61 72
PPV6 CAM AF	FUNC_TEST=TRUE	61 72
PPV9 CAM	FUNC_TEST=TRUE	61 72

POWER - OTHER

PPV8 ALWAYS	FUNC_TEST=TRUE	61 72
PPBATT VCC	FUNC_TEST=TRUE	60 65 69 72
PPLED OUT A	FUNC_TEST=TRUE	61 72
PPLED OUT B	FUNC_TEST=TRUE	61 72
PPV25 GRAPE	FUNC_TEST=TRUE	61 72
PPV8 XTAL	FUNC_TEST=TRUE	11
PPVCC MAIN	FUNC_TEST=TRUE	60 61 64 65 72
PPBATT POS RC	FUNC_TEST=TRUE	61 72
PPV0 LCM VBOOST	FUNC_TEST=TRUE	61 63
PPVBUS USB DCIN	FUNC_TEST=TRUE	65 72
PPVBUS PROT	FUNC_TEST=TRUE	25 65
VBUS PROT G	FUNC_TEST=TRUE	65

POWER - CAMERA (FRONT)

PPV2 CAM FRONT FILT	FUNC_TEST=TRUE	20 21
PPV8 CAM FRONT FILT	FUNC_TEST=TRUE	20 21
PPV9 AVDD CAM FRONT FILT	FUNC_TEST=TRUE	20 21

POWER - CAMERA (REAR)

PPV25 CAM REAR FILT	FUNC_TEST=TRUE	20 21
PPV8 CAM REAR FILT	FUNC_TEST=TRUE	20 21
PPV6 CAM REAR AF FILT	FUNC_TEST=TRUE	20 21
PPV9 AVDD CAM REAR FILT	FUNC_TEST=TRUE	20 21

POWER - AUDIO

PPV8 DMIC MIC FILT	FUNC_TEST=TRUE	23
PPV8 DMIC BTN FILT	FUNC_TEST=TRUE	28
PPV7 VCP	FUNC_TEST=TRUE	22
PPVBOOST R	FUNC_TEST=TRUE	24
PPVBOOST L	FUNC_TEST=TRUE	24

POWER - SENSORS

PPV8 COMPASS	FUNC_TEST=TRUE	18
PPV8 PHOS FILT	FUNC_TEST=TRUE	18
PPV8 OSCAR FILT	FUNC_TEST=TRUE	17
PPV2 OSCAR FILT	FUNC_TEST=TRUE	17
PPV0 GYRO FILT	FUNC_TEST=TRUE	18
PPV0 SENSOR PROX FILT	FUNC_TEST=TRUE	58

POWER - DISPLAY

PPVCC MAIN LCD SW CONN	FUNC_TEST=TRUE	31 32
PPVCC MAIN LCD SW	FUNC_TEST=TRUE	32

POWER - MESA

PPV825 S2R MESA FILT	FUNC_TEST=TRUE	31 33
PPV1 S2R MESA FILT	FUNC_TEST=TRUE	31 33
PPV1V3 MESA FILT	FUNC_TEST=TRUE	31 33

POWER - GRAPE

PPVDD STINGER BOOST	FUNC_TEST=TRUE	29
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POWER - BACKLIGHT

PPLED BACK REG A	FUNC_TEST=TRUE	31 32
LED IO 1 A	FUNC_TEST=TRUE	31 63
LED IO 2 A	FUNC_TEST=TRUE	31 63
LED IO 3 A	FUNC_TEST=TRUE	31 63
LED IO 4 A	FUNC_TEST=TRUE	31 63
LED IO 5 A	FUNC_TEST=TRUE	31 63
LED IO 6 A	FUNC_TEST=TRUE	31 63
PPLED BACK REG B	FUNC_TEST=TRUE	31 32
LED IO 1 B	FUNC_TEST=TRUE	31 63
LED IO 2 B	FUNC_TEST=TRUE	31 63
LED IO 3 B	FUNC_TEST=TRUE	31 63
LED IO 4 B	FUNC_TEST=TRUE	31 63
LED IO 5 B	FUNC_TEST=TRUE	31 63
LED IO 6 B	FUNC_TEST=TRUE	31 63

SOC - JTAG/RESET

JTAG SOC SEL	FUNC_TEST=TRUE	4 5
JTAG SOC TCK	FUNC_TEST=TRUE	5 25
JTAG SOC TDI	FUNC_TEST=TRUE	5 25
JTAG SOC TMS	FUNC_TEST=TRUE	5 25
TP JTAG SOC TEST L	FUNC_TEST=TRUE	4 5
TP JTAG SOC TDO	FUNC_TEST=TRUE	4 5
SOC TESTMODE	FUNC_TEST=TRUE	4 5
RESET SOC L	FUNC_TEST=TRUE	4 5 10 25 62 68 70
GPIO FORCE DFU	FUNC_TEST=TRUE	6 67

SOC - UART

UART SOC2DEBUG TX	FUNC_TEST=TRUE	6 25
UART DEBUG2SOC TX	FUNC_TEST=TRUE	6 25

SOC - USB

USB SOC N	FUNC_TEST=TRUE	5 25
USB SOC P	FUNC_TEST=TRUE	5 25

E75

E75 ACC DET CONN L	FUNC_TEST=TRUE	25 27
PPVBUS E75 USB CONN	FUNC_TEST=TRUE	24 27 69
PPOUT E75 ACC ID1 CONN	FUNC_TEST=TRUE	26 27
PPOUT E75 ACC ID2 CONN	FUNC_TEST=TRUE	26 27
E75 DPAIR1 CONN N	FUNC_TEST=TRUE	25 27
E75 DPAIR1 CONN P	FUNC_TEST=TRUE	25 27
E75 DPAIR2 CONN N	FUNC_TEST=TRUE	25 27
E75 DPAIR2 CONN P	FUNC_TEST=TRUE	25 27

AUDIO - HEADPHONE

CONN HP HEADSET DET FILT	FUNC_TEST=TRUE	22 23
CONN HP HS3 FILT	FUNC_TEST=TRUE	22 23
CONN HP HS3 REF FILT	FUNC_TEST=TRUE	22 23
CONN HP HS4 FILT	FUNC_TEST=TRUE	22 23
CONN HP HS4 REF FILT	FUNC_TEST=TRUE	22 23
CONN HP LEFT FILT	FUNC_TEST=TRUE	22 23
CONN HP RIGHT FILT	FUNC_TEST=TRUE	22 23
GPIO SOC2AJ HS3 SHUNT EN FILT	FUNC_TEST=TRUE	23
GPIO SOC2AJ HS4 SHUNT EN FILT	FUNC_TEST=TRUE	23

AUDIO - SPEAKER AMPS

SPKRAMP L OUT N	FUNC_TEST=TRUE	24 27 70
SPKRAMP L OUT P	FUNC_TEST=TRUE	24 27 70
SPKRAMP R OUT N	FUNC_TEST=TRUE	24 27 70
SPKRAMP R OUT P	FUNC_TEST=TRUE	24 27 70

AUDIO - CODEC

AIN3P	FUNC_TEST=TRUE	22
AIN3N	FUNC_TEST=TRUE	22
GPIO CODEC2PMU HS IRO L	FUNC_TEST=TRUE	22 62 70
GND AUDIO CODEC	FUNC_TEST=TRUE	22
MIKEY TS P	FUNC_TEST=TRUE	22 25
MIKEY TS N	FUNC_TEST=TRUE	22 25

AUDIO - DIGITAL MICS

DMIC MIC SCLK	FUNC_TEST=TRUE	22 23
DMIC BTN SCLK	FUNC_TEST=TRUE	22 28

BUTTONS

GPIO BTN HOME CONN L	FUNC_TEST=TRUE	31 33
GPIO BTN ONOFF L	FUNC_TEST=TRUE	5 6 23 62
GPIO BTN VOL UP L FILT	FUNC_TEST=TRUE	28
GPIO BTN VOL DOWN L FILT	FUNC_TEST=TRUE	28

NAND

ANC0 CE0 L	FUNC_TEST=TRUE	7 16 70
ANC1 CE0 L	FUNC_TEST=TRUE	7 16 70

BATTERY

BATT SWI CONN	FUNC_TEST=TRUE	66
BATT NTC	FUNC_TEST=TRUE	62 66
BATT SNS	FUNC_TEST=TRUE	65 66

GRAPE

CLK SOC2GRAPE 32K	FUNC_TEST=TRUE	9 30 70
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BASEBAND

BOUNDARY SCAN EN	FUNC_TEST=TRUE	35 39
GPIO PMU2BBPMU RESET L	FUNC_TEST=TRUE	62 68 70 71
GPIO SOC2BB RADIO ON L	FUNC_TEST=TRUE	6 68 71
HSIC BB2SOC RESET RDY	FUNC_TEST=TRUE	6 68
GPIO BB2SOC RESET DET L	FUNC_TEST=TRUE	6 68
HSIC BB2SOC DEVICE RDY	FUNC_TEST=TRUE	6 68
GPIO SOC2BB RESET L	FUNC_TEST=TRUE	6 68
GPIO PMU2BB VBUS DET	FUNC_TEST=TRUE	62 68 71
GPIO BB2PMU HOST WAKE L	FUNC_TEST=TRUE	62 68 70

BASEBAND - POWER

PP LDO6	FUNC_TEST=TRUE	35 36 71 73
PP LDO13	FUNC_TEST=TRUE	36 38 55 73
VREG SMP51 OV90	FUNC_TEST=TRUE	36 38
VREG SMP53 OV95	FUNC_TEST=TRUE	36 73

BASEBAND - SIM CARD

PP LDO5 FILT	FUNC_TEST=TRUE	59
SIMCRD RST CONN FILT	FUNC_TEST=TRUE	59 71
SIMCRD CLK CONN FILT	FUNC_TEST=TRUE	59 71
SIMCRD IO CONN FILT	FUNC_TEST=TRUE	59 71
SIMCRD DETECT FILT	FUNC_TEST=TRUE	59 71

WIFI/BT

GPIO PMU2BT REG ON	FUNC_TEST=TRUE	57 62 68 70
GPIO PMU2WLAN REG ON	FUNC_TEST=TRUE	57 62 68 70
CLK PMU2WLAN 32K	FUNC_TEST=TRUE	57 62 68 70

CAMERA - REAR

ISP CAM REAR CLK F	FUNC_TEST=TRUE	20 21
ISP CAM REAR SCL F	FUNC_TEST=TRUE	20 21
ISP CAM REAR SDA F	FUNC_TEST=TRUE	20 21
ISP CAM REAR SHUTDOWN L F	FUNC_TEST=TRUE	20 21

CAMERA - FRONT

ISP CAM FRONT CLK F	FUNC_TEST=TRUE	20 21
ISP CAM FRONT SCL F	FUNC_TEST=TRUE	20 21
ISP CAM FRONT SDA F	FUNC_TEST=TRUE	20 21
ISP CAM FRONT SHUTDOWN L F	FUNC_TEST=TRUE	20 21

MESA

GPIO MESA2SOC IRO FILT	FUNC_TEST=TRUE	31 33
MESA BOOST ENABLE FILT	FUNC_TEST=TRUE	31 33
SPI MESA MISO FILT	FUNC_TEST=TRUE	31 33
SPI MESA MOSI FILT	FUNC_TEST=TRUE	31 33
SPI MESA SCLK FILT	FUNC_TEST=TRUE	31 33

HALL EFFECT

GPIO HALL2PMU IRO0	FUNC_TEST=TRUE	19 62
GPIO HALL2PMU IRO1 FILT	FUNC_TEST=TRUE	29 30
PPV0 S2R GRAPE HALL FILT	FUNC_TEST=TRUE	29 30

ALS

PPV0 MIC ALS FILT	FUNC_TEST=TRUE	23
PPV0 HP ALS FILT	FUNC_TEST=TRUE	23
GPIO HP ALS2SOC IRO L FILT	FUNC_TEST=TRUE	23
GPIO MIC ALS2SOC IRO L F	FUNC_TEST=TRUE	23

I2C HP ALS SCL I1V8 FILT

I2C HP ALS SCL I1V8 FILT	FUNC_TEST=TRUE	23 70
I2C HP ALS SDA I1V8 FILT	FUNC_TEST=TRUE	23 70
I2C MIC ALS SCL I1V8 F	FUNC_TEST=TRUE	23 70
I2C MIC ALS SDA I1V8 F	FUNC_TEST=TRUE	23 70

DISPLAY

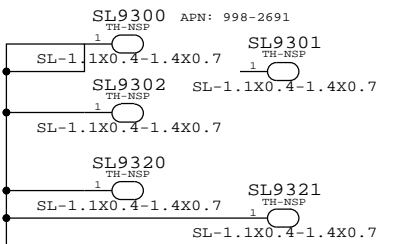
EDP HPD EMI	FUNC_TEST=TRUE	32
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OSCAR

CLK PMU2OSCAR 32K AND RESET L	FUNC_TEST=TRUE	17 62 70
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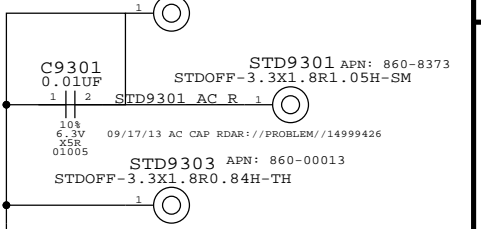
SOCHOT0 L

SOCHOT0 L	FUNC_TEST=TRUE	6 62
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FOREHEAD B2B STANDOFFS

STD9300	APN: 860-8373
STDOFF-3.3X1.8R1.05H-SM	

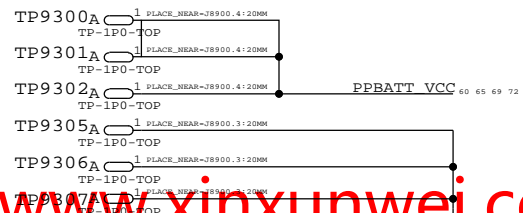
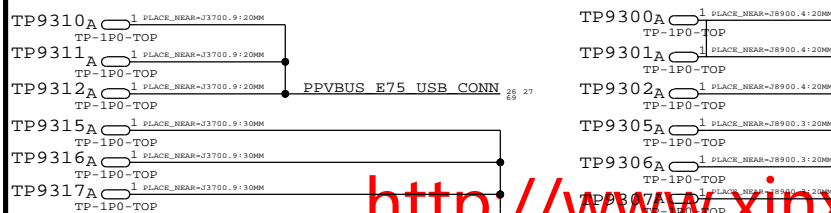
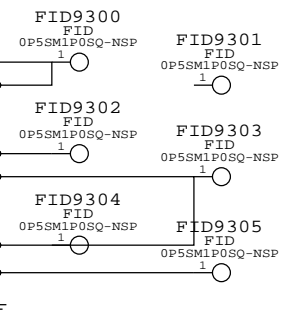
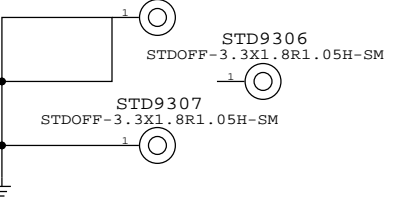


BUTTON FLEX B2B STANDOFFS

STD9302	APN: 860-8373
STDOFF-3.3X1.8R1.05H-SM	

GRAPE AND DISPLAY B2B STANDOFFS

STD9305	APN: 860-8373
STDOFF-3.3X1.8R1.05H-SM	



## DEV BOARD NET TERMINATION

NC SOC GPIO09	NO_TEST=TRUE	MAKE_BASE=TRUE	GPIO ALS2SOC DEVBRD IRO L	6
NC PMU GPIO20	NO_TEST=TRUE	MAKE_BASE=TRUE	GPIO DEVBRD2PMU WAKE L	62
NC ULPI STP	NO_TEST=TRUE	MAKE_BASE=TRUE	GPIO SOC2DEVBRD S3E WAKE	6
NC ULPI DATA3	NO_TEST=TRUE	MAKE_BASE=TRUE	GPIO SOC2DEVBRD S3E RESET2 L	6
NC PCIE CLKREQ2	NO_TEST=TRUE	MAKE_BASE=TRUE	PCIE DEVBRD2SOC CLKREQ L	6
NC PCIE PERST2	NO_TEST=TRUE	MAKE_BASE=TRUE	PCIE SOC2DEVBRD RESET L	6
NC NAND SYS CLK	NO_TEST=TRUE	MAKE_BASE=TRUE	CLK SOC2DEVBRD PCIE 24MHZ	6
NC I2S4 MCK	NO_TEST=TRUE	MAKE_BASE=TRUE	GPIO DISPLAY ID0	6
NC I2S5 MCK	NO_TEST=TRUE	MAKE_BASE=TRUE	GPIO DISPLAY ID1	6

SYNC MASTER=N/A		SYNC DATE=N/A	
PAGE TITLE			
TEST: TPS/HOLES/FIDUCUALS			
Apple Inc.		DRAWING NUMBER	051-0301
		REVISION	B.0.0
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# EE CHARACTERIZATION TP

## SOC

PP9501	1	RESET SOC L	PLACE_SIDE=TOP	4 5 10 25 62 68 69
PP9503	1	SOCHOT0 L R		62
PP9503	1	TP GPIO DFU STATUS	FUNC_TEST=TRUE	6

PP9502	1	TP ANALOGMUXOUT		5
--------	---	-----------------	--	---

PP9507	1	PPVDD CPU SOC SENSE	PLACE_NEAR=U0600.AB13:1.5MM	13 62
PP9508	1	PPVDD GPU SOC SENSE	PLACE_NEAR=U0600.N26:1.5MM	13 62
PP9588	1	PPVDD SRAM SOC SENSE	PLACE_NEAR=U0600.N25:1.5MM	13 62
PP9513	1	PPVDD SOC SOC SENSE	PLACE_NEAR=U0600.N25:1.5MM	13 62





PP9509	1	TP SOC VSS SENSE	PLACE_NEAR=U0600.M26:1.5MM	12
PP9510	1	TP SOC VSS CPU SENSE	PLACE_NEAR=U0600.AC13:1.5MM	12

ANCO AD<1..7>	FUNC_TEST=TRUE	7 16
ANCO CR0 L	FUNC_TEST=TRUE	7 16 69
ANCO ALE	FUNC_TEST=TRUE	7 16
ANCO CLE	FUNC_TEST=TRUE	7 16
ANCO WE L	FUNC_TEST=TRUE	7 16
ANCO RE L	FUNC_TEST=TRUE	7 16

ANC1 AD<0>	FUNC_TEST=TRUE	7 16
ANC1 CR0 L	FUNC_TEST=TRUE	7 16 69
ANC1 ALE	FUNC_TEST=TRUE	7 16
ANC1 CLE	FUNC_TEST=TRUE	7 16
ANC1 WE L	FUNC_TEST=TRUE	7 16
ANC1 RE L	FUNC_TEST=TRUE	7 16
ANC1 DOS	FUNC_TEST=TRUE	7 16

PPVREF ANC SOC	FUNC_TEST=TRUE	7
PPVREF ANC NAND	FUNC_TEST=TRUE	7
NAND SLOTO RDYBSY L	FUNC_TEST=TRUE	16

PP9505	1	ANCO AD<0>	PLACE_SIDE=BOTTOM	7 16
PP9506	1	ANCO DOS	PLACE_SIDE=BOTTOM	7 16
PP9500	1	GND	(PLACE_SIDE=TOP)	7 16
PP9504	1	=PP1V8 NAND	(PLACE_SIDE=TOP)	16 72
PP9500	1	TP ANC TCKC NAND	(PLACE_SIDE=TOP)	16
PP9504	1	TP ANC TMSC NAND	(PLACE_SIDE=TOP)	16

PMU			
	GPIO PMU2BBPMU RESET L	FUNC_TEST=TRUE	62 68 69
	GPIO BT2PMU HOST WAKE	FUNC_TEST=TRUE	57 62 68
	GPIO BB2PMU HOST WAKE L	FUNC_TEST=TRUE	62 68 69
	GPIO CODEC2PMU HS IRO L	FUNC_TEST=TRUE	22 62 69

CLK PMU2WLAN 32K	FUNC_TEST=TRUE	57 62 68 69 70
CLK PMU2OSCAR 32K AND RESET	FUNC_TEST=TRUE	17 62 69

PA NTC P	FUNC_TEST=TRUE	62 68
BOARD TEMP2 P	FUNC_TEST=TRUE	62
BOARD TEMP3 P	FUNC_TEST=TRUE	62
BOARD TEMP4 P	FUNC_TEST=TRUE	62
BOARD TEMP5 P	FUNC_TEST=TRUE	62
BOARD TEMP6 P	FUNC_TEST=TRUE	62
BOARD TEMP7 P	FUNC_TEST=TRUE	62
BOARD TEMP8 P	FUNC_TEST=TRUE	62

TP BUCK LDO UOV	FUNC_TEST=TRUE	62
TP BUCK SLDP MUX	FUNC_TEST=TRUE	62

TP AMUX AY	FUNC_TEST=TRUE	62
TP AMUX BY	FUNC_TEST=TRUE	62

PP9511	1	DWI SOC2PMU CLK		6 62
PP9512	1	DWI SOC2PMU DO		6 62
PP95F1	1	SYS ALIVE		62

## GRAPE

I2C GRAPE SDA 1V8	FUNC_TEST=TRUE	29 30
TP JTAG CUMULUS M TCK	FUNC_TEST=TRUE	76
TP JTAG CUMULUS M TDI	FUNC_TEST=TRUE	76
JTAG CUMULUS M TMS	FUNC_TEST=TRUE	76
SPI GRAPE SCLK	FUNC_TEST=TRUE	6 30
SPI GRAPE MISO	FUNC_TEST=TRUE	6 30
SPI GRAPE MOSI	FUNC_TEST=TRUE	6 30
SPI GRAPE CS L	FUNC_TEST=TRUE	6 30
GPIO SOC2GRAPE RESET L	FUNC_TEST=TRUE	6 30
GPIO GRAPE2SOC IRO L	FUNC_TEST=TRUE	6 30
DISPLAY SYNC	FUNC_TEST=TRUE	6 30
CLK SOC2GRAPE 32K	FUNC_TEST=TRUE	9 30 69
CUMULUS M2S CLK	FUNC_TEST=TRUE	30
CUMULUS M2S SDA	FUNC_TEST=TRUE	30
I2C GRAPE SDA 1V8	FUNC_TEST=TRUE	29 30 70
I2C GRAPE SCL 1V8	FUNC_TEST=TRUE	29 30

PP9514	1	TP CUMULUS S CS L		30
PP9515	1	TP CUMULUS S GPIO 3		30

## AUDIO

DMIC MIC SD	FUNC_TEST=TRUE	22 23
DMIC BTN SD	FUNC_TEST=TRUE	22 23
GPIO CODEC2SOC IRO L	FUNC_TEST=TRUE	6 22

TP9500 A	TP-P5	SPKRAMP R OUT P	FUNC_TEST=TRUE	24 27 69
TP9501 A	TP-P5	SPKRAMP R OUT N	FUNC_TEST=TRUE	24 27 69
TP9502 A	TP-P5	SPKRAMP R OUT N	FUNC_TEST=TRUE	24 27 69
TP9503 A	TP-P5	SPKRAMP R OUT N	FUNC_TEST=TRUE	24 27 69
TP9510 A	TP-P5	SPKRAMP L OUT P	FUNC_TEST=TRUE	24 27 69
TP9511 A	TP-P5	SPKRAMP L OUT P	FUNC_TEST=TRUE	24 27 69
TP9512 A	TP-P5	SPKRAMP L OUT N	FUNC_TEST=TRUE	24 27 69
TP9513 A	TP-P5	SPKRAMP L OUT N	FUNC_TEST=TRUE	24 27 69

PP95D0	1	I2S SOC2SPKRAMP MCK		6 24
PP95D1	1	I2S SOC2SPKRAMP BCLK		6 24
PP95D2	1	I2S SOC2SPKRAMP LRCK		6 24
PP95D3	1	I2S SOC2SPKRAMP DOUT		6 24
PP95D4	1	I2S SPKRAMP2SOC DOUT		6 24

PP95D7	1	I2S SOC2CODEC ASP MCK		6 22
PP95D8	1	I2S SOC2CODEC ASP BCLK		6 22
PP95D9	1	I2S SOC2CODEC ASP LRCK		6 22
PP95DA	1	I2S SOC2CODEC ASP DOUT		6 22
PP95DB	1	I2S CODEC2SOC ASP DOUT		6 22
PP95DC	1	I2S SOC2CODEC XSP BCLK		6 22
PP95DD	1	I2S SOC2CODEC XSP LRCK		6 22
PP95DE	1	I2S SOC2CODEC XSP DOUT		6 22
PP95DF	1	I2S CODEC2SOC XSP DOUT		6 22

CAMERA - FRONT				
PP9520	1	MIPI CAM FRONT CLK P	PLACE_NEAR=U0600.AV36:1.5MM	8 21 70
PP9521	1	MIPI CAM FRONT CLK N	PLACE_NEAR=U0600.AV36:1.5MM	8 21 70
PP9522	1	MIPI CAM FRONT DATA P<0>	PLACE_NEAR=U0600.AV37:1.5MM	8 21 70
PP9523	1	MIPI CAM FRONT DATA N<0>	PLACE_NEAR=U0600.AV37:1.5MM	8 21 70
CAMERA - REAR				
PP9524	1	MIPI CAM REAR CLK P	PLACE_NEAR=U0600.AV31:1.5MM	8 21 70
PP9525	1	MIPI CAM REAR CLK N	PLACE_NEAR=U0600.AV31:1.5MM	8 21 70
PP9526	1	MIPI CAM REAR DATA P<0>	PLACE_NEAR=U0600.AV31:1.5MM	8 21 70
PP9527	1	MIPI CAM REAR DATA N<0>	PLACE_NEAR=U0600.AV31:1.5MM	8 21 70

## OSCAR

PP95C0	1	TP OSCAR P0 05		17
PP95C1	1	TP OSCAR P0 06		17
PP95C2	1	TP OSCAR P0 09		17
PP95C3	1	TP OSCAR P0 17		17
PP95C4	1	TP OSCAR P0 21		17
PP95C8	1	TP OSCAR P1 02		17
PP95C9	1	TP OSCAR P1 03		17
PP95CD	1	SWD OSCAR IO 1V8		9 17
PP95CE	1	SWD OSCAR CLK 1V8		9 17

## CHAN 0 NEAR DRAM

PP9534	1	DDR0 CK P	PLACE_NEAR=U1600.W13:1.5MM	14 70
PP9535	1	DDR0 CK N	PLACE_NEAR=U1600.W13:1.5MM	14 70
PP9536	1	DDR0 CKE<0>	PLACE_NEAR=U1600.W14:1.5MM	14 70
PP9537	1	DDR0 CA<0>	PLACE_NEAR=U1600.W17:1.5MM	14 70
PP9538	1	DDR0 CA<1>	PLACE_NEAR=U1600.W17:1.5MM	14 70
PP9539	1	DDR0 CA<2>	PLACE_NEAR=U1600.W16:1.5MM	14 70
PP9540	1	DDR0 CA<3>	PLACE_NEAR=U1600.W16:1.5MM	14 70
PP9541	1	DDR0 CSN<0>	PLACE_NEAR=U1600.W14:1.5MM	14 70
PP9542	1	DDR0 CSN<1>	PLACE_NEAR=U1600.W14:1.5MM	14 70

PP9530	1	DDR0 DOS P<0>	PLACE_NEAR=U1600.D15:1.5MM	14 70
PP9531	1	DDR0 DOS N<0>	PLACE_NEAR=U1600.D14:1.5MM	14 70
PP9532	1	DDR0 DQ<0>	PLACE_NEAR=U1600.C17:1.5MM	14 70

## CHAN 0 NEAR SOC

PP9570	1	DDR0 DOS P<0>	PLACE_NEAR=U0600.D7:1.5MM	14 70
PP9571	1	DDR0 DOS N<0>	PLACE_NEAR=U0600.D6:1.5MM	14 70
PP9572	1	DDR0 DQ<0>	PLACE_NEAR=U0600.D13:1.5MM	14 70

## CHAN 1 NEAR DRAM

PP9542	1	DDR1 DOS P<0>	PLACE_NEAR=U1600.K4:1.5MM	70
PP9543	1	DDR1 DOS N<0>	PLACE_NEAR=U1600.K4:1.5MM	70
PP9544	1	DDR1 DQ<0>	PLACE_NEAR=U1600.K3:1.5MM	70

## CHAN 1 NEAR SOC

PP9572	1	DDR1 DOS P<0>	PLACE_NEAR=U0600.V1:1.5MM	14 70
PP9573	1	DDR1 DOS N<0>	PLACE_NEAR=U0600.U1:1.5MM	14 70
PP9574	1	DDR1 DQ<0>	PLACE_NEAR=U0600.AA3:1.5MM	14 70

## WIFI

TP JTAG WLAN TMS	FUNC_TEST=TRUE	68
TP JTAG WLAN TRST	FUNC_TEST=TRUE	68
JTAG WLAN SEL	(TD1) FUNC_TEST=TRUE	57
UART SOC2WLAN RTS L	(TD0) FUNC_TEST=TRUE	6 57 68
WLAN SECI IN	FUNC_TEST=TRUE	57

OSCAR2RADIO CONTEXT A	FUNC_TEST=TRUE	57 68
OSCAR2RADIO CONTEXT B	FUNC_TEST=TRUE	57 68
UART BT2SOC TX	FUNC_TEST=TRUE	6 68
UART SOC2BT TX	FUNC_TEST=TRUE	6 57
UART SOC2WLAN TX	FUNC_TEST=TRUE	6 57 68
UART WLAN2SOC TX	FUNC_TEST=TRUE	6 68
UART BB2WLAN COEX RX	FUNC_TEST=TRUE	40 57 71
UART WLAN2BB COEX TX	FUNC_TEST=TRUE	40 57
I2S SOC2BT BCLK	FUNC_TEST=TRUE	6 57 68
I2S SOC2BT LRCK	FUNC_TEST=TRUE	6 57 68
I2S BT2SOC DOUT	FUNC_TEST=TRUE	6 68
I2S SOC2BT DOUT	FUNC_TEST=TRUE	6 57 68
CLK PMU2WLAN 32K	FUNC_TEST=TRUE	57 62 68 69 70
GPIO PMU2WLAN REG ON	FUNC_TEST=TRUE	57 62 68 69
GPIO PMU2BT REG ON	FUNC_TEST=TRUE	57 62 68 69
GPIO WLAN2PMU HOST WAKE	FUNC_TEST=TRUE	57 62 68 69
GPIO BT2PMU HOST WAKE	FUNC_TEST=TRUE	57 62 68 69
GPIO SOC2WLAN WAKE	FUNC_TEST=TRUE	57 62 68 69
GPIO SOC2BT WAKE	FUNC_TEST=TRUE	57 62 68 69

## OTHER PPS

PP95B8	1	WLAN GPIO 8		57
PP95B9	1	WLAN GPIO 10		57
PP95B3	1	WLAN GPIO 11		57

I2C				
I2C OSCAR2PROX SDA 1V8	FUNC_TEST=TRUE	17 58		
I2C OSCAR2PROX SCL 1V8	FUNC_TEST=TRUE	17 58		
I2C0 SCL 1V8	FUNC_TEST=TRUE	4 6		
I2C0 SDA 1V8	FUNC_TEST=TRUE	4 6		
I2C1 SCL 1V8	FUNC_TEST=TRUE	4 6		
I2C1 SDA 1V8	FUNC_TEST=TRUE	4 6		
I2C2 SCL 1V8	FUNC_TEST=TRUE	4 6		
I2C2 SDA 1V8	FUNC_TEST=TRUE	4 6		

PP95F4	1	=I2C3 SDA 1V8		4
PP95F5	1	=I2C3 SCL 1V8		4

I2C HP ALS SCL 1V8 FILT	FUNC_TEST=TRUE	23 69
I2C HP ALS SDA 1V8 FILT	FUNC_TEST=TRUE	23 69
I2C MIC ALS SCL 1V8 F	FUNC_TEST=TRUE	23 69
I2C MIC ALS SDA 1V8 F	FUNC_TEST=TRUE	23 69

## UART

UART SOC2ACC TX	FUNC_TEST=TRUE	25
UART ACC2SOC TX	FUNC_TEST=TRUE	25
UART SOC2OSCAR TX	FUNC_TEST=TRUE	17
UART OSCAR2SOC TX	FUNC_TEST=TRUE	17

## CHAN 2 NEAR DRAM

PP9548	1	DDR2 CK P	PLACE_NEAR=U1700.W13:1.5MM	10 15 70
PP9549	1	DDR2 CK N	PLACE_NEAR=U1700.W13:1.5MM	10 15 70
PP9550	1	DDR2 CKE<0>	PLACE_NEAR=U1700.W14:1.5MM	10 15 70
PP9551	1	DDR2 CA<0>	PLACE_NEAR=U1700.V17:1.5MM	10 15 70
PP9552	1	DDR2 CA<1>	PLACE_NEAR=U1700.W17:1.5MM	10 15 70
PP9553	1	DDR2 CA<2>	PLACE_NEAR=U1700.V16:1.5MM	10 15 70
PP9554	1	DDR2 CA<3>	PLACE_NEAR=U1700.W16:1.5MM	10 15 70
PP9555	1	DDR2 CSN<0>	PLACE_NEAR=U1700.V14:1.5MM	10 15 70
PP9556	1	DDR2 CSN<1>	PLACE_NEAR=U1700.V14:1.5MM	10 15 70

PP9545	1	DDR2 DOS P<0>	PLACE_NEAR=U1700.D15:1.5MM	10 15 70
PP9546	1	DDR2 DOS N<0>	PLACE_NEAR=U1700.D14:1.5MM	10 15 70
PP9547	1	DDR2 DQ<0>	PLACE_NEAR=U1700.C17:1.5MM	10 15 70

## CHAN 2 NEAR SOC

PP9585	1	DDR2 DOS P<0>	PLACE_NEAR=U0600.AM1:1.5MM	10 15 70
PP9586	1	DDR2 DOS N<0>	PLACE_NEAR=U0600.AM1:1.5MM	10 15 70
PP9587	1	DDR2 DQ<0>	PLACE_NEAR=U0600.AM3:1.5MM	10 15 70

## CHAN 3 NEAR DRAM

PP9556	1	DDR3 DOS P<0>	PLACE_NEAR=U1700.K4:1.5MM	10 15 70
PP9557	1	DDR3 DOS N<0>	PLACE_NEAR=U1700.L4:1.5MM	10 15 70
PP9558	1	DDR3 DQ<0>	PLACE_NEAR=U1700.K3:1.5MM	10 15 70

## CHAN 3 NEAR SOC

PP9596	1	DDR3 DOS P<0>	PLACE_NEAR=U0600.AT10:1.5MM	10 15 70
PP9597	1	DDR3 DOS N<0>	PLACE_NEAR=U0600.AT11:1.5MM	10 15 70
PP9598	1	DDR3 DQ<0>	PLACE_NEAR=U0600.AP7:1.5MM	10 15 70

## SOC SIDE PCIE TPS

PP95A7	1	PCIE WLAN2SOC TX C P		9 68 70
PP95A8	1	PCIE WLAN2SOC TX C N		9 68 70
PP95A9	1	PCIE SOC2WLAN TX P		9 57 68 70
PP95B0	1	PCIE SOC2WLAN TX N		9 57 68 70
PP95B1	1	PCIE SOC2WLAN CLK P		9 57 68 70
PP95B2	1	PCIE SOC2WLAN CLK N		9 57 68 70
PP95B3	1	PCIE SOC2WLAN RESET		9 57 68 70

## WLAN SIDE PCIE TPS

PP95A7	1	PCIE WLAN2SOC TX C P		9 68 70
PP95A8	1	PCIE WLAN2SOC TX C N		9 68 70
PP95A9	1	PCIE SOC2WLAN TX P		9 57 68 70
PP95B0	1	PCIE SOC2WLAN TX N		9 57 68 70
PP95B1	1	PCIE SOC2WLAN CLK P		9 57 68 70
PP95B2	1	PCIE SOC2WLAN CLK N		9 57 68 70
PP95B3	1	PCIE SOC2WLAN RESET		9 57 68 70






















## REMOVED PCIE SOC2WLAN TX C P PP BECAUSE THE IT BLOCKED THE SHIM RING.


## REMOVED PCIE SOC2WLAN TX C N PP BECAUSE THE P VERSION WAS REMOVED

## REMOVED PCIE SOC2WLAN TX C P PP BECAUSE THE P VERSION WAS REMOVED

## REMOVED PCIE SOC2WLAN TX C N PP BECAUSE THE P VERSION WAS REMOVED

RF TEAM REQUESTED TPS

	SIMCRD_RST_CONN_FILT	FUNC_TEST=TRUE	59	69
	SIMCRD_CLK_CONN_FILT	FUNC_TEST=TRUE	59	69
	SIMCRD_IO_CONN_FILT	FUNC_TEST=TRUE	59	69
	SIMCRD_DETECT_FILT	FUNC_TEST=TRUE	59	69
	PP_LDO6	FUNC_TEST=TRUE	35	36 69 73
	UART_BB2SOC_TX	FUNC_TEST=TRUE	6	25 68
	UART_SOC2BB_TX	FUNC_TEST=TRUE	6	25 68
	UART_BB2SOC_RTS_L	FUNC_TEST=TRUE	6	68
	UART_SOC2BB_RTS_L	FUNC_TEST=TRUE	6	68
	UART_OSCAR2BB_TX	FUNC_TEST=TRUE	17	68
	UART_BB2OSCAR_TX	FUNC_TEST=TRUE	17	68
	UART_BB2WLAN_COEX_RX	FUNC_TEST=TRUE	40	57 70
	UART_WLAN2BB_COEX_TX	FUNC_TEST=TRUE	40	57 70
	GPIO_SOC2BB_WAKE_MODEM	FUNC_TEST=TRUE	6	68
	GPIO_BB2SOC_GPS_SYNC	FUNC_TEST=TRUE	6	68
	USB_BB_P	FUNC_TEST=TRUE	25	68
	USB_BB_N	FUNC_TEST=TRUE	25	68
	GPIO_SOC2BB_COREDUMP	FUNC_TEST=TRUE	6	68
	GPIO_SOC2BB_RADIO_ON_L	FUNC_TEST=TRUE	6	68 69
	GPIO_PMU2BBPMU_RESET_L	FUNC_TEST=TRUE	62	68 69 70
	GPIO_PMU2BB_VBUS_DET	FUNC_TEST=TRUE	62	68 69
PP9600	SN	1	HSIC_BB_DATA	5 68
P4MM	SN	1	HSIC_BB_STB	5 68
PP9601	SN	1	HSIC_BB_STB	5 68
P4MM	SN	1	HSIC_BB_STB	5 68

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 Apple Inc.		DRAWING NUMBER	051-0301
		REVISION	B.0.0
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
1	225V	PP_LDO1	36 38 42 43
1	8V	PP_LDO2	36 38
1	8V	PP_LDO3	36 37 38 55
3	075V	PP_LDO4	36 38
2	85V	PP_LDO5	36 38 59
2	85V	PP_LDO6	35 36 69 71
1	9V	PP_LDO7	36 38 40
2	05V	PP_LDO8	36 42 43
1	2V	PP_LDO9	36 38
0	9V	PP_LDO10	36 38
1	8V	PP_LDO11	35 36 38 39 40 42 43 44
0	95V	PP_LDO12	36 38
2	95V	PP_LDO13	36 38 55 69
2	95V	PP_LDO13_GPS	55
2	7V	PP_LDO14_RFSW	36 46 47
0	95V	VREG_SMPS3_0V95	36 69
2	075V	VREG_SMPS4_2V075	36

0	9V	PP_VSW_S1	36
1	25V	PP_VSW_S2	36
0	95V	PP_VSW_S3	36
2	075V	PP_VSW_S4	36

4	7V	PP_BATT_VCC	35 44 53 68
4	7V	PP_VCC_MAIN	73
4	2V	PP_BATT_VCC_2GPA	45
4	2V	PP_BATT_VCC_QPOET	44 45 50 51
4	2V	PP_BATT_VCC_RADIO	35 36
4	7V	PP_BATT_VCC_DSM	53
4	2V	PP_BATT_VCC_QPOET_HBS	51
4	2V	PP_BATT_VCC_QPOET_ASM	50

1	8V	PP_1V8_S2R_VDDIO_WLAN_BT	57 68
1	8V	PP_WL_VDDIO	57
4	7V	PP_VCC_MAIN	73

0V	S1_GND	36
0V	S2_GND	36
0V	S3_GND	36
0V	S4_GND	36
0V	GND_SW	44
0V	VOUT_BOOST_GND	44

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